High-κ Oxides

by E. L. Silva and M. C. Santos

Abstract

Due to the need of increasing the gate capacitance of metal-oxide-semiconductor (MOS) devices, the layer thickness of the SiO_2 gate dielectric is reducing to such thickness that the leakage current is becoming too large to control. Suitable high-κ oxides hence need to be found in order to replace the existing gate dielectric, because the thicker layer of the oxide contender may exponentially decrease the tunnelling currents, while achieving the same level of capacitance as the actual devices of SiO_2.

The layer thickness of insulating gate oxide in silicon MOS devices is decreasing to its size limits. This is due to the scaling-down of the electronic devices in order to increase the respective gate capacitance (capacitance scales as $C \sim \kappa/d$, where κ is the relative permittivity and d the oxide thickness). Because of this scale reduction, the thickness of the SiO_2 dielectric is currently decreasing to such thin layers that the gate leakage current (direct tunnelling of electrons through the material) is very high, allowing for the dissipation power to be uncontrollably high.

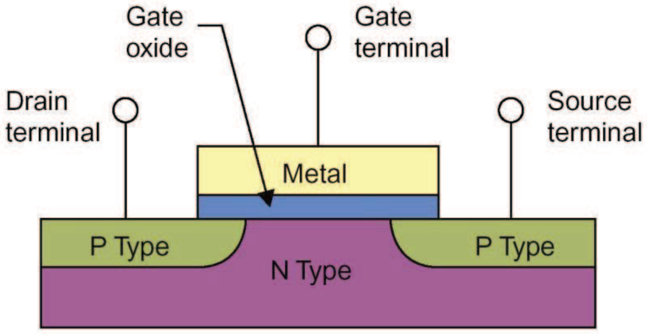

Figure 1 - Cross-section of a MOS transistor showing gate, body, source and drain terminals. The gate is separated from the body by an insulating oxide layer (figure from [3]).

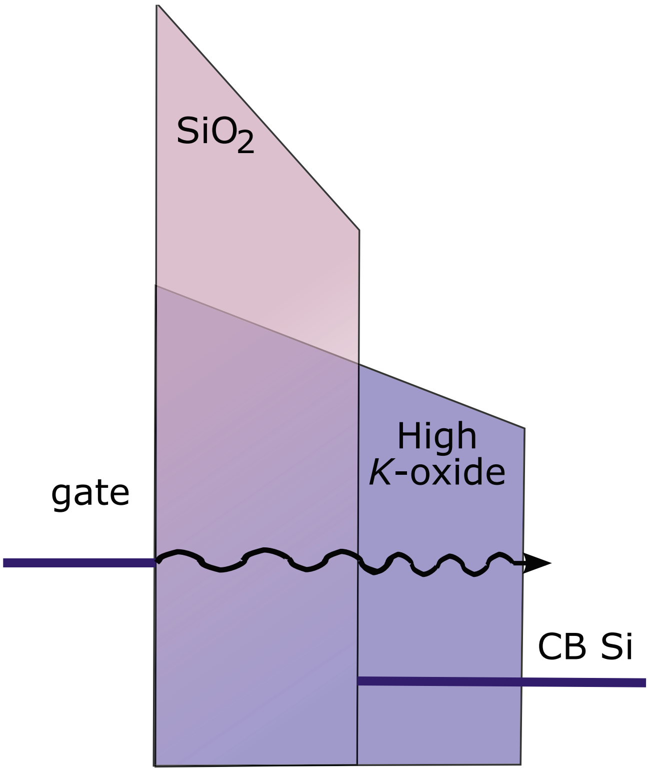

Figure 2 - Schematic of direct tunnelling through a SiO_2 layer and comparison of the tunnelling effect through a thicker layer of high κ oxide.

Suitable contenders to replace SiO_2, obeying specific requirements, need therefore to be found. One of the most important requirement is that the suitable contender has to posses a high dielectric constant, as mentioned previously[1]. This value has to be high enough to ensure the scaling-down of the electronic devices for a few more years. One the other hand, another requirement that the oxide contender must satisfy is that it must also act as an insulator, with band offsets with the adjoining Si channel of over 1 eV. This fact is to ensure that the carrier injection is minimized into its bands by acting as potential barriers [1, 2]. There is however a drawback regarding this fact. The width of the oxides band-gap vary inversely with the κ value. Hence, the choice of the oxide has to be done mainly by taking into account these two characteristics mutually, which makes the choice of the κ value to be lower than expected - see fig. 3.

Other important requirements that the oxide contender must satisfy is that it also needs to have good thermodynamically stability in contact to the Si channel, inhibiting the formation of thin insulating layers at the interface [1] and it has to have the highest electrical interface quality with few electronic defects.

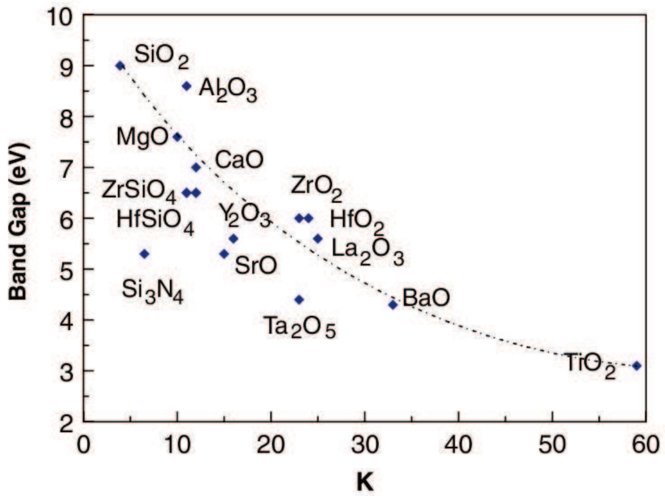

Figure 3 - Band-gap width as a function of the κ constant for gate oxides contenders (figure from ref. [1]).

Silica (SiO_2) is the most used oxide for gate-oxides because of the advantage of being a natural oxide layer and can easily be formed from silicon through oxidation, thus giving a good Si-oxide interface. The bonding between the Si atoms and O atoms are of covalent nature and therefore the defect density is low. Existing defects are mainly broken bonds or dangling bonds. SiO_2, being an amorphous oxide and being of low coordination (each Si has four O neighbours), existing defects can be easily removed due to interface bonding rearrangements.

High-κ oxides exhibit poorer performance than SiO_2, having higher concentration of bulk defects and a poorer interface with Si [4]. The high-κ oxides are mostly ionic oxides and these have different character of defects than SiO_2. As these oxides possess higher coordination number, the defect density is therefore higher [4]. The main defects found in ionic oxides are vacancies and interstitials, being the oxygen (O) vacancy probably the most important to focus upon because it is the main source for electron trapping [4]. Charge trapping can give rise to bias instability, low carrier mobility due to the charge scattering and gate threshold shifts, which degrade the reliability of the devices [5].

To continue Moore's law for next decades, the use of new materials for the implementation of high-κ gate dielectrics that can replace SiO_2, may allow further miniaturization of microelectronic components. Also, the need to identify such defects is crucial in order to choose the most favourable growth and processing O environment to minimize defect concentration. This can be achieved by altering the O partial pressure, therefore inducing the formation or suppression of such defects [5].

References

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[5] J. Robertson, K. Xiong and S. J. Clark, Defects in High-κ Gate Dielectric Stacks, p. 175, Springer (2006).

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