escola superior de tecnologia e gestão
instituto politécnico de leiria

Dissertação

Mestrado em Engenharia Eletrotécnica - Eletrónica e Telecomunicações

End-to-end 5G testbed characterisation and improvements at 60GHz

Luís Eduardo de Sousa Sismeiro

Leiria, March 2018

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Master dissertation performed under the guidance of Professor Rafael Ferreira da Silva Caldeirinha from Escola Superior de Tecnologia e Gestão of Instituto Politécnico de Leiria, Professor Carlos Miguel Nogueira Gaspar Ribeiro from Escola Superior de Tecnologia e Gestão of Instituto Politécnico de Leiria, Professor Manuel García Sánchez from Universidade de Vigo, Spain, and Rodolfo Vitorino Gomes from University of South Wales, UK.

Leiria, March 2018

Acknowledgements

I would first like to thank all of my advisers Professor Rafael Caldeirinha, Professor Carlos Ribeiro, Professor Manuél Sanchéz and Rodolfo Gomes for all their help and disposition in guiding me to the conclusion of this work. I would also like to thank the University of Vigo for the funding of this work.

A thank you to all of the members of the research group of Antennas and Propagation'-Lr at Instituto de Telecomunicações Leiria for all their help and good work environment. A special thank you to Marco Santos and Sofia Gualdino from the Electronic Center for all their help in the development of the PCBs and availability throughout this project.

To my parents and sister for all their help throughout my academic life and for being there when I needed.

And finally, a special thank you to Beatriz Ferreira, without whom I would not be here today. Thank you for keeping my mind focused throughout these years and for being there whenever I needed you.

Abstract

Wireless communications for the next mobile generation, the 5G, are set to increase both throughput and reliability than what is currently seen in mobile systems. These are set to be able to cope with the increase in mobile subscribers that is bound to occur in the next years and with the increasing demand in data rates and lower latency for immediate access to high-volume data.

Therefore, this dissertation describes a characterization of a full end-to-end 5G testbed at 60 GHz capable of transmitting up to 1 Gbps. This characterization will evaluate the current state of the art of 60 GHz commercial front-end devices and compare it to a custom solution. This characterization evaluates both performance and Radio Frequency (RF) impairments. Furthermore, the baseband system is also evaluated in performance and signal impairments.

To conclude the performance evaluation of the commercial device, a real-world scenario was drawn and tested where this emulates an Augmented Reality (AR) wireless device and evaluates the feasibility of such system on a classroom environment. To scale this work and improve signal reliability, a Multiple-Input Multiple-Output (MIMO) Alamouti transmission and receiver diversity block code on System Generator was also devised and simulated .

Keywords: 60 GHz, Testbed, mmWave, augmented reality, MIMO.

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List of Acronyms

AC	Alternated Current
ADC	Analogue to Digital Converter
AGC	Automatic Gain Control
ASIC	Application Specific Integrated Circuit
AR	Augmented Reality
BER	Bit Error Rate
BPSK	Binary Phase Shift Keeying
CDF	Cumulative Distributive Function
CFO	Carrier Frequency Offset
CI	Clock Input
COTS	Commercial-Off-The-Shelf
DAC	Digital to Analogue Converter
DC	Direct Current
DFT	Discrete Fourier Transform
DL	Downlink
DSP	Digital Signal Processor
EIRP	Equivalent Isotropic Radiated Power
eMBB	enhanced Mobile Broadband
ENOB	Effective Number Of Bits
EVM	Error Vector Magnitude
f_c	Centre Frequency

FPGA Field Programmable Gate Array

GPP General Purpose Processors

GPU Graphics Processing Unit

GUI Guide User Interface

HMD Head Mounted Display

I In-phase

ICI Intercarrier Interference

ISI Intersymbol Interference

IT Instituto de Telecomunicações

ITU International Telecommunications Union

LNA Low-Noise Amplifier

LO Local Oscillator

MIMO Multiple-Input Multiple-Output

MISO Multiple-Input Single-Output

mmWave Millimetre Wave

mMTC massive Machine Type Communication

OFDM Orthogonal Frequency Division Multiplexing

OHMD Optical Head Mounted Display

PA Power Amplifier

PAM Pulse Amplitude Modulation

PAPR Peak-to-Average Power Ratio

PC Personal Computer

PCB Printed Circuit Board

PLL Phase Lock Loop

PN Phase Noise

Q Quadrature

QAM Quadrature Amplitude Modulation

QoS Quality-of-Service

QPSK Quadrature Phase-Shift Keeing

RF Radio Frequency

RMS Root Mean Square

ROM Read-only Memory

RX Receiver

SA Spectrum Analyser

SD Spatial Diversity

SDR Software Defined Radio

SFDR Spurious Free Dynamic Range

SIMO Single-Input Multiple-Output

SINAD Signal-to-Noise+Distortion Ratio

SISO Single-Input Single-Output

SM Spatial Multiplexing

SNIR Signal-to-Noise+Interference Ratio

SNR Signal-to-Noise Ratio

SOC System-on-a-Chip

STBC Space-Time Block Code

TX Transmitter

UE User Equipment

UL Uplink

uMTC ultra-Reliable Machine-Type Communication

USB Universal Serial Bus

USW University of South Wales

VGA Variable Gain Amplifier

VR Virtual Reality

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Chapter 1

Introduction

1.1 Motivation

The 5G, the next mobile communications generation, is expected to finally bring millimetre wave (mmWave) devices to the mobile sector. The free bandwidth available at 60 GHz, in particular, as long been thought as a solution for the high data rate requirements for the 5G [1]. However, components at such high frequency induce severe impairments that limit the overall system performance. These non-idealities can affect both transmitted and received radio signals. For that reason, a characterisation of the impairments and solutions to prevent or reduce their impact are required in the design of transmission schemes.

Furthermore, the increase in throughput in wireless systems will flourish and evolute current and future technologies such as immersive media, i.e. Virtual Reality (VR) and Augmented Reality [2]. These are seen as the future in a variety of sectors such as entertainment, health care and education [3]. Education AR systems in particular have been studied as a way to improve students learning by virtually inserting complex objects, such as magnetic fields, for the student to see and interact. Immersive technologies have shown for the last decade to have finally overcome its early limitations and are currently able to meet its public expectations [4]. However, to fully make use of these technologies, these must become wireless. Although currently wireless devices for both systems do exist, their capabilities are lacking the ones achieved with wired ones. Moreover, to fully immerse the user in the virtual world created in these devices, increasingly higher resolution and detail will be designed for this end. As such, 5G mmWave systems may present as solution to this problem.

Following the current trend in increasing mobile users [5], the need for a system capable of both coping with One of the main technologies that will flourish thanks to the increase in wireless data rates in the 5G is the immersive media, such as Virtual Reality (VR) and Augmented Reality [2]. These technologies have been gathering interest in recent years [4] and

1.2 Objectives

In this dissertation, a characterisation of a RF complete system is presented, from baseband to RF up and down-conversion impairments. Furthermore, a real case scenario is tested to validate this system as capable of meeting next mobile communications generation requirements. It is presented a spatial diversity MIMO code for the expansion of the current system. The main objectives of this work are described as following:

- Characterise the impairments on baseband and RF front-ends;
- Characterise the performance of a custom and a commercially available RF Front-end;
- Develop a real case measurement scenario;
- Expansion to Alamouti Receiver Diversity MIMO through a System Generator design block.

1.3 Structure of the document

This document is divided in six chapters, where the first chapter pertains to the current introduction to the developed work, with its motivation and objectives. The following five chapters are divided as follows:

The second chapter gives an overview of the state of the art in 5G technology, from what technologies will be used to its verticals and final uses. Furthermore, a summary of developed testbeds and trials is given, both past and future. On the third chapter, a theoretical overview of the different concepts used in this work is given, with a technical explanation and examples of the impact of certain RF impairments on a given signal. The fourth chapter presents the characterization performed on the

available 5G testbed system, with measurements of performance done on two types of RF front-end, a custom and a commercial solution. In the fifth chapter, a real case scenario is presented and tested for a classroom AR system with wireless data transmission. This system is measured for multiple users and for different channel multipath scenarios. The sixth chapter presents a MIMO block code developed in System Generator. This block can be implemented on the present work and improve both transmitter and receiver diversity. The final chapter presents the conclusions and future work for this dissertation. It is also presented the literature contributions resulting from this work.

Chapter 2

State of Art

The next mobile communications generation, the 5G, is expected to start being deployed by 2020 [1]. While previous generations were driven by service or technology requirements, the 5G aims to be the driving force behind technology evolution [6]. In [1], the International Telecommunication Union (ITU) sets three major group sectors that will benefit from the 5G. These are: enhanced Mobile Broadband (eMBB), ultra-reliable Machine-Type Communication (uMTC), and massive Machine Type Communication (mMTC), as seen in figure 2.1.

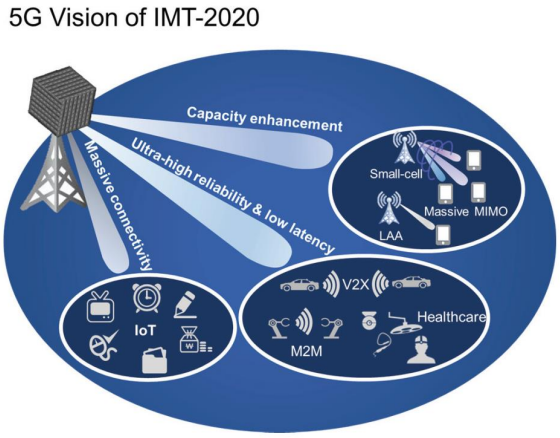


Figure 2.1: 5G vision of IMT 2020, from [7].

The eMBB will focus on the user experience, with ultra high-definition content, such as AR and VR, transmitted at **high speed** and low latency within a **hotspot** connection in a high user density and low mobility area. As for the wider area coverage, data rates will increase in comparison with current generations, although lower than in more urban areas. uMT, on the other hand, envisions the industrial manufacturing, remote medical surgery and autonomous vehicles cases, where high data rate and low

latency networks are of the utmost importance. As for the mMTC, small low-cost devices associated with the Internet-of-Things (IoT) will be used to perform less delay sensitive communications, with short periodical data bursts in order to maximize battery lifetime. These however will be present in higher scale than the previous cases and therefore will require support for a higher number of devices.

2.1 5G roadmap

For every new mobile communications generation, a group of steps are devised to develop and mature the new technologies associated. For the 5G, the growth in both mobile users and data consumption forecast for the next decade determined the need for a new system capable of coping with this increased capacity [5]. Therefore, a set of 5G requirements have been introduced in [1, 3, 8]. These are summarized as:

- Peak data rate of 20 Gbps;
- Data rates of 100 Mbps in metropolitan areas;
- Data rates of 1 Gbps to simultaneous users in the same office floor;
- Hundreds of thousands of connected wireless sensors;
- Enhanced spectral efficiency when compared to 4G;
- 99.9% area coverage;
- 1 ms end-to-end latency.

To meet these requirements, new technologies have been thought out to be introduced in the 5G. Two core technologies that will set the 5G apart from previous mobile networks are mmWave signals and MIMO [1, 3, 9, 10, 11].

mmWaves are signals at frequencies between 30 and 300 GHz, which translates to a wavelength of 10 and 1 millimetre, respectively. Although mmWave signals have been thought as an exciting solution for mobile communications for a number of years, limitations in chip manufacturing brought this idea to a halt. Currently however, newer processes in semiconductors design have allowed them to have the high-speed, low-power consumption and low-cost for large-scale manufacturing [12]. Furthermore, throughout the world, an agreement for the free licensing of spectrum at the mmWave

band makes this an appealing solution for the 5G. In particular, the 60 GHz band has been gathering interest as the band for high speed close-quarters communications, such as indoor. This interest has been exacerbated with newer IEEE standards on this frequency band, such as IEEE 802.15.3c [13] (the first gigabit wireless communications standard), the IEEE 802.11.ad [14] and more recently the IEEE 802.11.ay [15]. For example, 802.11.ad compliant devices have been introduced in the market recently, with routers [16] and laptop computers [17] available for high-bandwidth wireless communications. mmWave signals, however, suffer from higher signal path loss then previous sub-6GHz communications. As such, implementations of other techniques to improve resilience to signal fading are of the utmost importance, with massive MIMO presenting as a solution to this problem.

MIMO technology is described as an array of antennas on both transmitter and receiver side working as one. This technology can improve signal spectrum efficiency when compared with traditional SISO systems, with two main techniques employed for the data transmission: Spatial Diversity (SD) and Spatial Multiplexing (SM) [18]. Due to the multipath fading, the transmitted signals may suffer phase shifts, attenuation or distortion. Therefore, to improve signal reliability, SD is employed. SD systems transmit the same information through the multiple antennas to improve both transmission and receiver diversity, i.e. improve the system robustness to multipath fading. SM, on the other hand, splits the information through the transmitting antennas to improve the system's capacity. This method works by assuming that the high multipath scattering in the propagation environment makes the channel spatially selective and therefore each receiving antenna will only receive its intended data stream. A summary of these techniques is shown in figure 2.2.

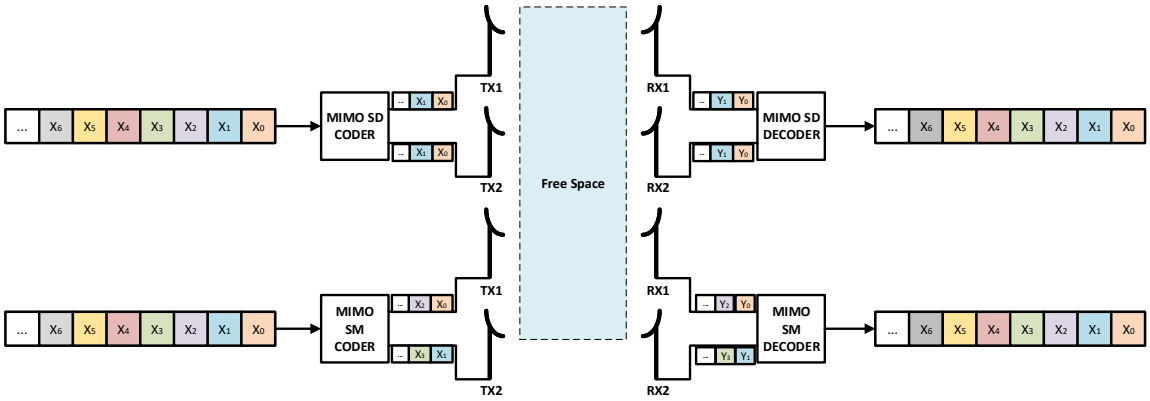


Figure 2.2: MIMO techniques: Spatial Diversity (SD) and Spatial Multiplexing (SM).

Massive MIMO can be described as large-scale MIMO and it is able to support multiple users in the same time-frequency by employing sub-sets of MIMO arrays to

each user. This grants advantages in spectrum efficiency and brings robustness to channel fading [19]. For example, in [20], a Massive MIMO system for the 5G is capable of reaching a spectral efficiency of 79.82 bps/Hz, more than two times higher than what is currently achieved with MIMO LTE-Advanced [21].

Immersive technologies, such as AR and VR, stand to benefit from 5G increased data rate and lower latency. VR and AR devices are seen as game-changers for future content consumption [22]. According to the top trends in Gartner's Hype Cycle for Emerging technologies in 2017 [23], VR and AR have now surpassed their peak of expectations and are reaching what is known as the slope of enlightenment (figure 2.3). This stage is characterized by the moment where the technology has surpassed its peak in inflated expectations and can now mature and be more widely understood. As such, VR and AR are being presented as a solution for a number of industry verticals for the 5G, from health care to entertainment and education [3]. AR devices in education, in particular, are intended to play an even more important role on the reduction of the student's average learning curve [24].

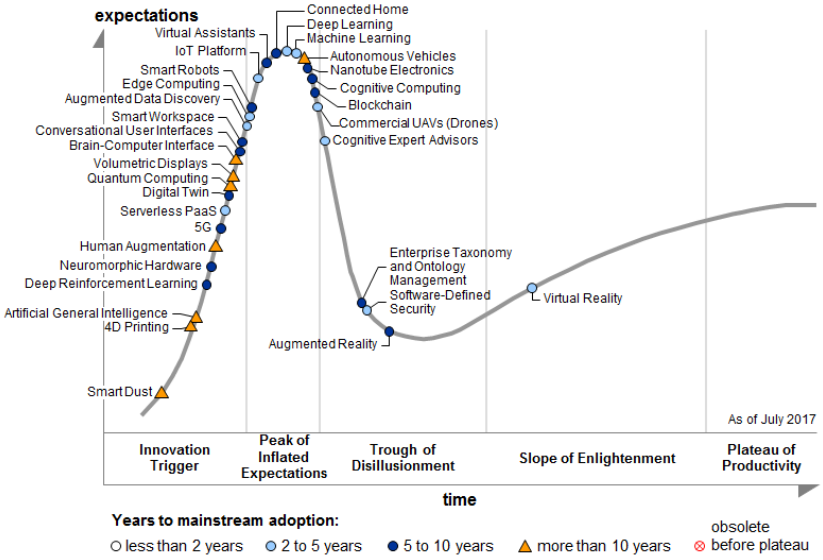


Figure 2.3: Gartner's Hype Cycle for Emerging Technologies, from [23].

AR transparent Optical Head Mounted Displays (OHMD) devices give the user a live view of virtual elements in a real world environment scenario, which makes this concept a mixed reality system. This can enhance human senses such as, visual, auditory, and haptic, from computer-generated perceptual information. Although similar, VR's occluded Head Mounted Displays (HMD) immerse the user in a virtual world, with no view of real objects. However, although these technologies have differing characteristics, the hardware processing unit specifications for both are similar. Both devices require the capability of providing high detail and frame-rate data to immerse

the user in the mixed/virtual world. Furthermore, low latency in both data transmission and Motion-to-Photon (MTP) - latency between user's head motion and the display update - are required to prevent what is known as simulation sickness. These requirements result in the need for a high throughput system between the AR/VR devices and the content generator. In the following table, the requirements for both immerse reality devices is shown. These can be then summed up as supporting video resolutions up to 16k, at least 90 frames-per-second (fps) and latencies lower than 20 ms between the server (source) and the OHMD/HMD device.

Table 2.1: Summary of the recommended VR and AR system specifications.

Specification	**VR**	**AR**
Screen	Occluded	Transparent
Display	HMD	OHMD
Main Application	Entertainment	Industry & Education
Environment	Virtual	Real & Virtual
6DoF‡	✓	✓
Frame Rate	$\geq$ 90 fps	$\geq$ 90 fps
Bit resolution	16	
MTP*	$\leq$ 20 ms	$\leq$ 15 ms
Video Resolution	Full HD/4k/ 8k/16k	Full HD/4k/ 8k/16k
Data Rate	200-1000 Mbps	200-1000 Mbps
Latency	$<$ 20 ms (end-to-end)	$<$ 20 ms (end-to-end)
Processing power	6000 GFLOPS	

(‡) 6 Degrees of Freedom: freedom of movement in a three-dimensional space.

(*) Motion-to-Photon: latency between user's motion and the display updates.

Current AR/VR devices are tethered or untethered to the data source. Tethered, or wired, devices enable a more immersive experience due to having the virtual objects graphical computation done outside the display, at the expense of user mobility. On the other hand, wireless devices allow for the user to move freely within its space but are not able to display content with the same quality and data rate as in wired devices due to constrictions in battery life-time and overheating constraints [2], from high power consumption of Graphical Processing Units (GPUs). To this extent, to overcome these

limitations, data transmission must be performed over the air. Still, even state-of-the-art wired and wireless devices struggle to cope with the previous AR/VR specifications [25, 26, 27, 28]. For example, a system with more than 16 bits per pixel, a frame rate of 120 Hz and supporting 8k display resolution per eye and a HEVC encoder [29] would require a data transmission rate higher than 509.6 Mbps, which is approximately x34 times more than the rate of stated-of-art VR wired HTC Vive model can deliver [27]. Thus, 5G networks are seen as the technology that will drive immerse reality devices to their true potential by mixing the mobility of wireless devices with the graphical computational capabilities of wired ones by allocating the graphical computation to an outsourced server that will wirelessly transmit the information to the AR and VR devices.

In order to meet both the requirements and the 2020 deployment date, a series of roadmaps have been traced, such as the one shown in figure 2.4. In this figure, the European roadmap for the 5G is established, with the beginning and ending dates for all stages of the 5G network creation. This establishes a first stage of small scale testbeds which then will generate the large scale trials. These serve as the working grounds for the deployment of the technology. For the European roadmap, in 2018, the early experiments (testbeds) are ending and allocating their knowledge and technology to the wide-scale trials [10]. These are set to occur until and a year after the first technology deployment in 2020. In particular, large crowd events, such as winter and summer olympics or world and european football championships are seen as the perfect setting to test and showcase 5G capabilities due to their high concentration of people and global appeal.

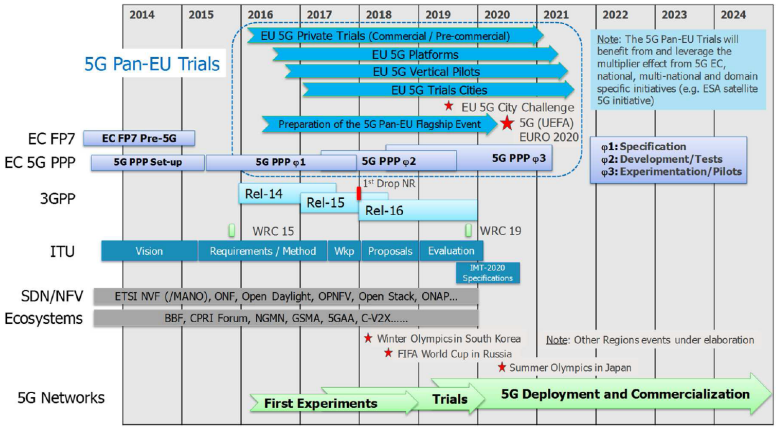


Figure 2: 5G Pan-EU Trials Roadmap

Figure 2.4: 5G Pan-Eu trials roadmap, from [10].

2.2 Existing testbeds for 5G

For the development of the technology for the 5G, in particular mmWave systems, a set of testbeds have been conducted in presented. Initial tests have been mainly deployed on an academic research setup while more recent setups introduced by technology enterprises and mobile service providers. To this extent, a literature overview of mmWave testbeds is presented next.

In an early stage, academic research conducted by universities showcased the early possibilities in testbeds at mmWave. In [30], a University of South Wales (USW) group conducted indoor measurements for two scenarios in the 60 GHz band using a Field Programmable Gate Array (FPGA) as the processing core and a single carrier transmission method. In it, a maximum throughput of 100 Mbps was reached with 16-Quadrature Amplitude Modulation (QAM). In [31], a group from Tokyo Institute of Technology compared their 10 Gbps Orthogonal Frequency Division Multiplexing (OFDM) with phase noise compensation system's specifications and performance to the ones in the IEEE norm 802.15.3c. This work made use of a FPGA as its data transmission memory and pass through to a Personal Computer (PC) for off-line processing. It transmitted through a 60 GHz cable connection employing 64-QAM as modulation.

More recently, 5G testbeds have evolved, with technology enterprises teaming-up with wireless service providers to conduct experiments. This is seen in [32], where Samsung and NTT DOCOMO, a Japanese wireless service provider, collaborated in measurements at 28 GHz on indoor and outdoor settings with Massive MIMO beamforming for a 2x2 MIMO antenna configuration on both transmitter and receiver to mitigate path loss. This system employed three modulations (Quadrature Phase Shift Keeying (QPSK),16-QAM,64-QAM) and achieved a maximum throughput of 1.2 Gbps. On the other hand, in [33], NTT DOCOMO partnered with Nokia for a beam-tracking proof-of-concept system for a small cell environment. This work achieved over 2 Gbps maximum throughput with Binary Phase Shift Keeying (BPSK), QPSK and 16-QAM modulation and is shown in the following figure.

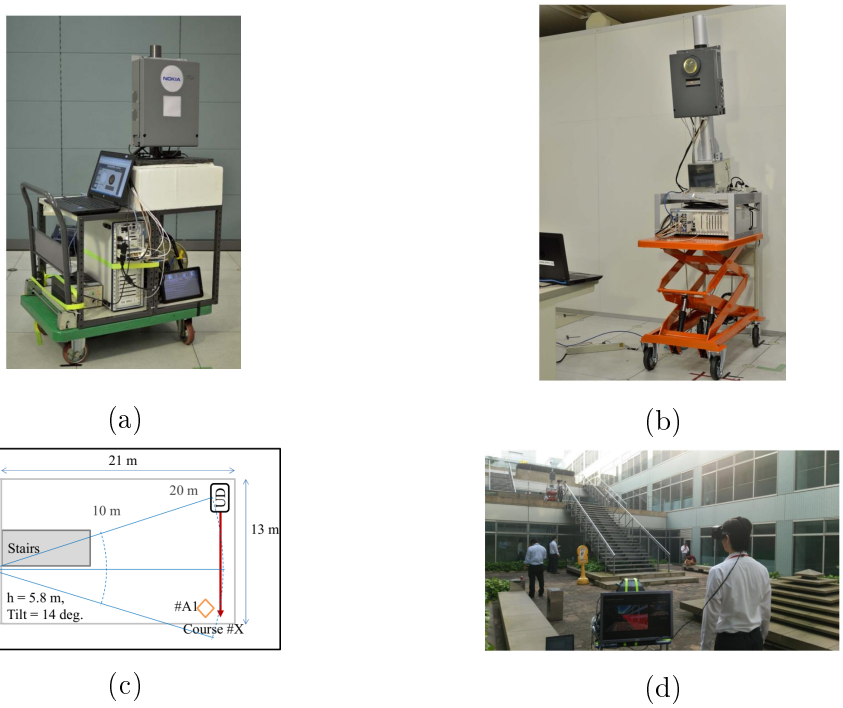


Figure 2.5: Measurement setup from [33]: (a) user device, (b) access point, (c) measurement course and (d) outdoor environment.

Other testbeds have been presented whether at 28 GHz or 60 GHz. In [34], 28 GHz measurements by NTT DOCOMO on moving vehicles in a speedway at 150 km/h were performed with an OFDM system with 64-QAM. This setup used Massive MIMO beamsteering antennas on both transmitter and receiver, with a 2x2 configuration in MIMO transmission and was capable of reaching 2.5 Gbps of wireless data rate. In [7], an Intermediate-Frequency-over-Fiber (IFoF) system is employed at 28 GHz. This system uses 64-QAM modulation with OFDM with one of the carriers transmitting the clock signal. This transmission of the clock signal was showed to not interfere with the system performance, with a maximum Error Vector Magnitude (EVM) error of 0.6%. As a result, this work was able to present a system capable of transmitting at 1 Gbps, in agreement with the 5G data rates. Finally, a 60 GHz testbed was shown in [35] where BPSK and 4-Pulse Amplitude Modulation (PAM) is used in a system capable of reaching 2.5 Gbps in a Line-of-Sight (LOS) MIMO setup.

In the following table, a summary of the previous mmWave testbeds is shown.

Table 2.2: Summary of current testbed mmWave systems.

Affiliation	Freq. Band [GHz]	Main Features					
		Transmission scheme	BW [GHz]	real-time	over the air	MAx. Spectral eff. [bit/s/Hz]	Max. SNR [dB]
USW	**60**	SC	0.035	yes	yes	4	28.5
Tokyo Institute of Technology	**60**	OFDM	2.16	no*	no	6	25.8
Samsung/ NTT DOCOMO	28	OFDM	0.8	yes	yes	4	21† / <28††
Nokia /NTT DOCOMO	73.5	SC	1	yes	yes	4	18
OpenMili	**60**	OFDM	0.0005	yes	yes	1	30
UESTC	**60**	SC	2.16	yes	yes	2	16.5
NTT DOCOMO	28	OFDM	0.8	N/A	yes	6	N/A
ONRGET	28	OFDM	0.125	yes	yes	6	28
HUB/UFAF	**60**	OFDM	0.625	no*	yes	1	N/A

(*) OFDM TX/RX processing is performed off-line by an host PC.
(†) Outdoor environment.
(††) Indoor environment.

2.3 First 5G trials

In the trial section for the 5G, the main goal is to present to the average consumer the possibilities available with the 5G. The first international 5G trial was conducted during the Winter Olympics in South Korea in 2018. This trial had demonstrations of self-driving buses, 360-degree real-time ultra high-definition virtual reality video from inside an ice hockey's player helmet or the implementation of digital networks through virtualization [36]. These trials employed Massive MIMO and signals at 28 GHz with 1 GHz bandwidth for the data transmission [37]

For future large-scale trials, the European Football Championship in 2020 is seen as the perfect platform to showcase and tune 5G systems [10]. This tournament will be played throughout 13 different European cities (Amsterdam, Baku, Bilbao, Brussels,

Bucharest, Budapest, Copenhagen, Dublin, Glasgow, London, Munich, Rome and Saint Petersburg) with the 5G trials set to impact three service stages: 5G augmented and virtual reality applications in and around the stadiums for the entertainment of the fans in immersive experiences; automated transportation to and from the stadiums to relevant transport routes, as for example to and from airports; face recognition augmented reality systems for public safety authorities. These trials will show to the public the capabilities of the 5G and and will be relevant for the future concept of Smart Cities. These however, will be dependent on agreements with each hosting city, with Amsterdam already showing interest in adopting these trials.

Chapter 3

Radio system design & performance evaluation

3.1 Introduction

To best understand the following work and what will be evaluated, an overview of the different referenced concepts is required. Thus, in the following chapter, a description of the different systems and measurements employed in this work are given.

3.2 Baseband level fundamentals

In the baseband level performance measurement, an evaluation of both processing unit and digital and analogue domain converters is required to best understand the system limitations. As such, in the following section, the different concepts that will be used in the following sections for baseband signals measurements are presented.

3.2.1 SDR and FPGA

A Software Defined Radio (SDR) does not have a concrete definition, although it can be described as a flexible radio waveform changed through software, without any hardware modifications [38]. This flexibility can turn a SDR in an ideal platform for new mobile communications testbeds and trials. A SDR includes both baseband processing and the conversion between both digital (baseband) and analogue (RF) domain. A SDR

transceiver block is shown in the following figure.

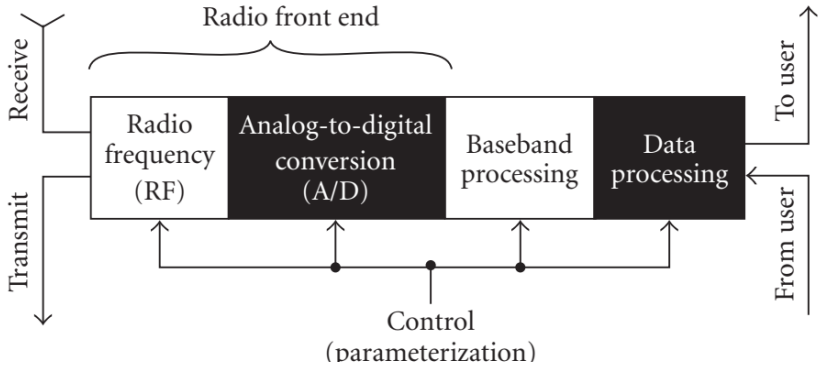


Figure 3.1: SDR transceiver, from [39].

For the data and baseband processing, three main devices can used: General Purpose Processors (GPPs), Digital Signal Processors (DSP) and FPGAs. The latter one, in particular, offers great flexibility and parallel processing which gives SDR developers the required reconfigurability for future wireless systems performance demands [40]. These systems are described as complex reconfigurable System-on-a-Chip (SOC) devices with configurable resource blocks (such as flip-flops, look-up tables and clock generation), multiple processor units and specialized Inputs/Outputs (I/O). Furthermore, for a later stage in the development of the SDR, an Application Specific Integrated Circuit (ASIC) can be configured from the resource blocks implemented on the FPGA.

3.2.2 DAC and ADC

Digital-to-analogue and analogue-to-digital converters (DAC/ADC) are one of the most important blocks in a SDR. These are responsible for making the bridge between the digital and the analogue states. In order to understand the hardware limitations in both analogue-to-digital and digital-to-analogue conversions, a series of measurements can be conducted to evaluate the converters performance. These are: the Signal-to-Noise+Distortion Ratio (SINAD), the Effective Number of Bits (ENOB) and the Spurious Free Dynamic Range (SFDR) [41]. A description of these measurements ensues, retrieved from [41, 42].

SINAD

SINAD describes the quality of a converter's dynamic range and it expresses the ratio between the analogue input signal to the noise and distortion, in dB. It is described by the following equation:

$$SINAD = 20\log_{10}\frac{A_{Signal}}{A_{Noise+Distortion}}, \tag{3.1}$$

where A_{Signal} is the root mean square (RMS) output signal and $A_{Noise+Distortion}$ is the RMS sum of all the spectral components under the Nyquist frequency. This value is dependent on both signal's frequency and amplitude.

ENOB

The ENOB gives the global accuracy of the bit resolution of the ADC for a given input and sampling rate, by comparing the RMS noise produced to the RMS noise of an ideal ADC with the same bit resolution. This is computed from the converter's digital data record as $N - log_2$ - where N is the number of digitized bits- of the ratio of measured and ideal RMS error:

$$ENOB = Nlog_2\Big(\frac{A_{MEASURED_{ERROR}}}{A_{IDEAL_{ERROR}}}\Big), \tag{3.2}$$

where $A_{MEASURED_{ERROR}}[rms]$ is the averaged noise and $A_{IDEAL_{ERROR}}[rms]$ is the quantization noise error, expressed as

$$\frac{q}{\sqrt{2}} = \frac{A_{FS}}{2N\sqrt{12}}. \tag{3.3}$$

ENOB can also be expressed from the ADC's full-scale input range amplitude (A_{FS}) to the reference voltage amplitude (A_{REF}):

$$ENOB = log_2\left(\frac{A_{FS}}{A_{MEASURED_{ERROR}}\sqrt{12}}\right) \tag{3.4}$$

or

$$ENOB = log_2\left(\frac{A_{REF}}{A_{MEASURED_{ERROR}}\sqrt{12}}\right) \tag{3.5}$$

ENOB can also be related to SINAD in dB and is generally expressed as:

$$ENOB = \frac{SINAD - 1.76}{6.02} \tag{3.6}$$

Therefore, ENOB is affected solely by noise, which can be originated from quantization error, AC/DC non-linearities, clock jitter and noise in the reference signal. Furthermore, this value is also dependent on the input signal's frequency and amplitude.

SFDR

Spurious Free Dynamic Range (SFDR) is defined as the usable dynamic range of a DAC before spurious noise interferes and/or distorts the fundamental signal, in dB. This describes the difference in amplitude between the fundamental signal and the largest harmonical or non-harmonical spur, from DC to the Nyquist bandwith ($f_s/2$, where f_s is the sampling frequency). In figure 3.2, an example of the measurement of SFDR is given.

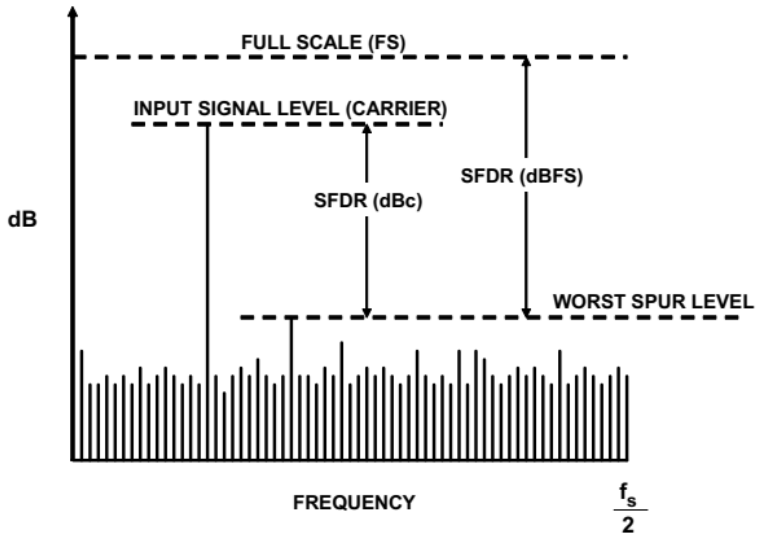


Figure 3.2: Spurious Free Dynamic Range measurement, from [42]

SFDR is measured from the RMS ratio of the fundamental signal's amplitude to the largest distortion component. In a well-designed system, this spur will come from a harmonic of the fundamental signal. This measurement is important so that an analysis of the noise and harmonics restrictions on the converter's dynamic range is performed.

Spurious-free dynamic range is the ratio of RMS amplitude of the fundamental (the maximum signal component) to the rms value of the largest distortion component in a specified frequency range. In well-designed systems, this spur should be a harmonic of the fundamental. SFDR is important because noise and harmonics restrict a data converter's dynamic range. In an IF bandpass converter, for example, spurs can be interpreted as adjacent channel information.

In pure sine-wave inputs, SFDR is described as the ratio of the amplitude of the averaged Discrete Fourier Transform (DFT) value at the fundamental frequency ($A[f_{IN}]$) to the amplitude of the averaged DFT value of the largest-amplitude harmonic distortion ($A_{HD_{MAX}}[rms]$) or spurious signal component ($A_{SPUR_{MAX}}[rms]$) observed over the Nyquist bandwidth.

$$SFDR[dBc] = 20log10\frac{|A[f_{IN}]|}{|A_{HD_{MAX}}|} \tag{3.7}$$

or

$$SFDR[dBc] = 20log10\frac{|A[f_{IN}]|}{|A_{SPUR_{MAX}}|} \tag{3.8}$$

In sum, SFDR is dependent on the amplitude and frequency of the input signal and as such, when measuring this value, these values must be specified.

3.2.3 DC Offset

Direct Current (DC) offset is a common occurence in direct-conversion systems. This can generate clipping on the ADC if not blocked by Alternated Current coupling at the ADC input. Due to some ADCs containing only DC coupling, this ADC saturation must be taken into account and the converter must provide high enough dynamic range to counter balance it.

3.2.4 Analogue AGC

An Automatic Gain Control (AGC) is a device that stabilizes an input signal to a specified output power [43]. This is composed of three main components: a Variable Gain Amplifier (VGA), an envelope detector and an integrator. This system works as follows: the input signal is amplified by the VGA. This signal is then passed through

the envelope detector that measures the envelope signal power of the VGA output signal. This is then compared to a reference voltage to produce a gain control voltage that is applied to the VGA to offset the amplification for the desired output power. This case is known as a feedback AGC. If the signal detection occurs at the input signal, with the VGA at the system's output, the AGC architecture is known as feedforward [44]. In figure 3.3, a diagram for these architectures is shown.

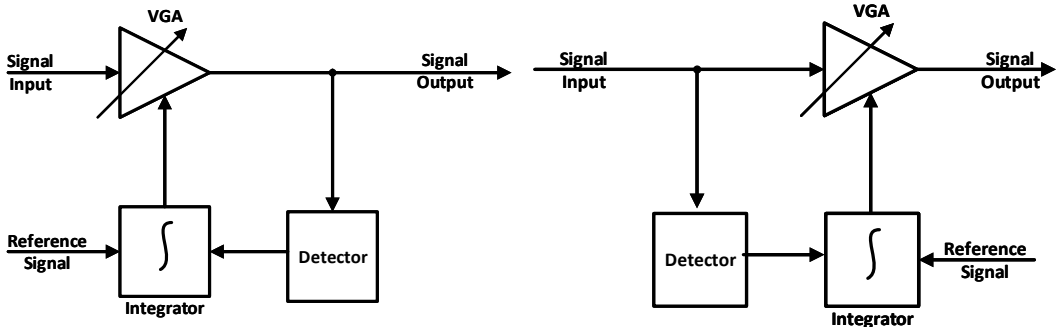


Figure 3.3: Analogue AGC architectures: Feedback (a) and Feedforward (b).

Both architectures present advantages and disadvantages depending on their final application, which are shown in table 3.1. The majority of these devices employ a feedback loop configuration since it is easier to design and does not require previous knowledge of the system specifications.

Table 3.1: Summary of main AGC architectures characteristics, from [44].

	Advantages	Disadvantages
Feedback Loop	• Low dynamic range at peak detector input • Higher linearity	• Instabilities with high compression or expansion • Slower settling time
Feedforward Loop	• No instability • Fast settling time	• Peak detector requires AGC's dynamic range • High linearity required for the loop

3.3 RF front-end fundamentals

3.3.1 Architectures

Homodyne

Homodyne architecture, also known as zero-IF, is a receiver structure that passes the RF signal at the carrier frequency to baseband signal at DC by a single mixing stage [45], as shown in figure 3.4. This architecture presents advantages to heterodyne mixers, such as: no Intermediate Frequency (IF) stage, no image-rejection filter and a lower number of components. However, this also presents some disadvantages, namely IQ imbalance and DC offset [46].

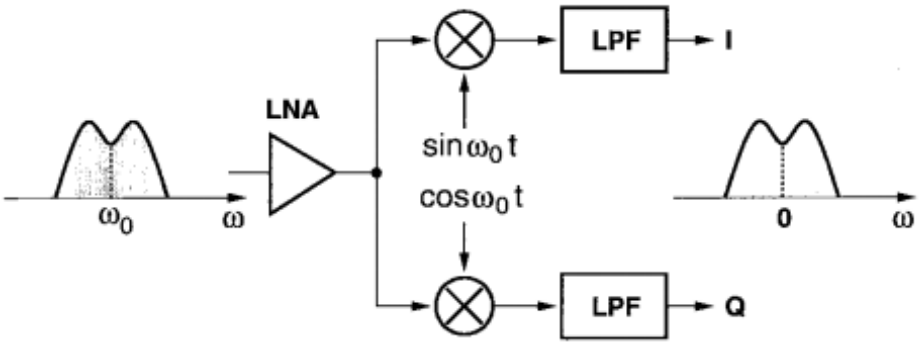


Figure 3.4: Homodyne mixer, from [46].

Heterodyne

The heterodyne receiver, in contrast with the homodyne structure, requires the RF signal to be translated to a low, non zero-IF, frequency where all the signal operations are performed. This results in two mixing operations occurring on a heterodyne receiver. The first mixer down-converts the RF signal to IF while the second one will translate the IF signal to baseband. While the IF stage can have several stages, on average this is only accomplished with one stage.

Furthermore, between mixing stages, an image selective filter is inserted, in order to suppress frequency images that could have impact on the following mixing stages [45, 47]. The resulting signal is then passed through a channel selective filter to obtain

the desired signal. Heterodyne receivers however also present disadvantages such as a higher number of components, namely extra mixers and LOs, and the need for high order image and channel selective filters.

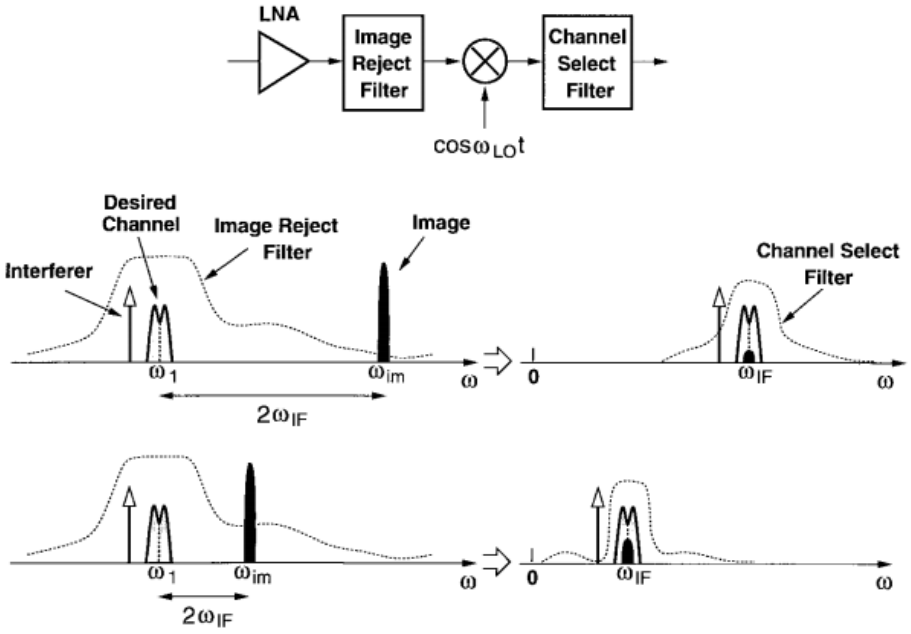


Figure 3.5: Heterodyne mixer, from [46].

3.3.2 RF impairments

Power Amplifier distortion

In a wireless communication system, a Power Amplifier (PA) is placed on a transmitter in order to improve the transmission power. This, however, is one of the most power-consuming blocks in a wireless communication device. Its efficiency determines the total system power consumption and therefore the device's battery life. It is given by the following equation

$$\eta = \frac{P_{RFout}}{P_{DCin} * P_{RFin}}, \tag{3.9}$$

where P_{RFout} is the transmission output power, P_{DCin} is the power delivered from the power supply and P_{RFin} is the incident RF power to the device. As with any other amplifier, PAs show non-linear behaviour and saturation gain at high input levels. In order to maximize its efficiency, the PA usually operates on the saturation region, thus increasing its non-linearities. Amplification of non-linear signals distorts the transmitted signal and in regards to OFDM symbols, this is specially important due to its high Peak-to-Average Power Ratio (PAPR). As such, when working with OFDM symbols,

the PA must work at an inefficient point of operation to reduce its non-linearities.

Linearity in PAs is usually characterized by two input power levels: P_{1dB} and $IIP3$. P_{1dB} represents the 1-dB compression point, that is, the input power level when the actual output power level is 1 dB lower than the ideal output power of an ideal power amplifier. On the other hand, the Third-order Intercept Point ($IIP3$) represents the point input power level at which two output versus input power characteristics intercept. In figure 3.6, these concepts are shown.

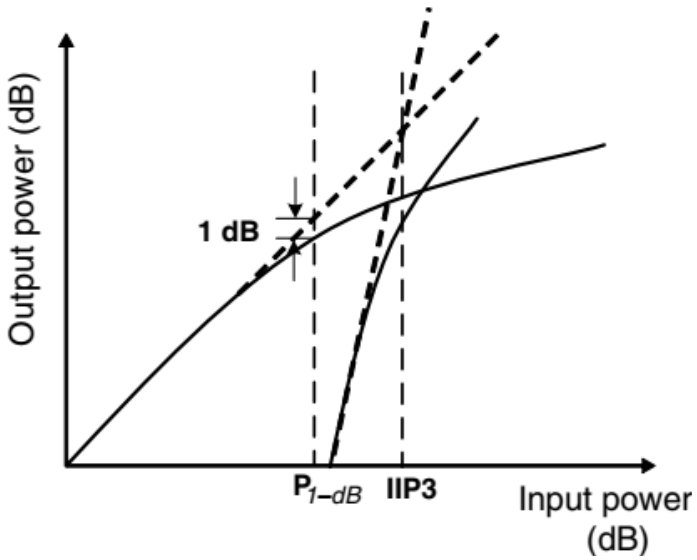


Figure 3.6: PA non-linearities, from [45]

Carrier Frequency Offset

Carrier Frequency Offset (CFO) arises when the carrier signal on the down-conversion at the receiver mixer is not synchronised with the Local Oscillator (LO). This can be attributed to two factors: frequency discrepancy between transmitter and receiver LOs and the Doppler effect when the transmitter and/or the receiver is moving. This results in a frequency shift on the received signal, as can be seen on figure 3.7.

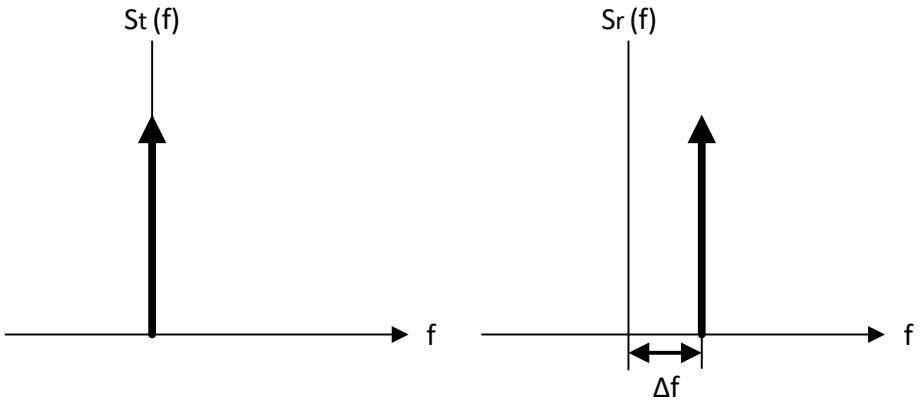


Figure 3.7: Signal transmitted ($S_t(f)$) and signal received ($S_r(t)$) with a frequency shift (Δf).

In OFDM systems, the synchronisation between transmitter and receiver LOs allows it to maintain the orthogonality between its sub-carriers. As such, if it occurs CFO between both LOs, the orthogonality is lost, causing Intercarrier Interference (ICI). In a real non-ideal system, CFO is always present and thus can only be minimized, by, for example, recurring to high stability LOs on both communication ends.

Phase Noise

Phase noise is commonly known as oscillator jitter. However, phase noise relates to the noise spectrum centred around the oscillation frequency in the frequency domain while jitter represents the precision of the oscillation periodicity in the time domain. Phase noise occurs due to the impossibility of oscillators to generate pure sinusoidal waves with impulsive spectra [45]. This creates a vestigial sideband around the oscillation frequency. Through a discrete-time Wiener-Levy process, the phase noise (θ_n) of a free running oscillator can be modeled in the time domain as such:

$$\theta_n(t_n) = \theta_n(t_n - 1) + \psi(t_n), \tag{3.10}$$

where $\psi(t_n)$ is an independent and identically distributed Gaussian-distributed random variable representing the phase increment at the time t_n with variance

$$\sigma_\psi^2 = 2\pi B T_s, \tag{3.11}$$

with B representing the two-sided 3-dB bandwidth and T_s the sampling interval. Therefore, the power spectral density of the local oscillator (LO) signal with such phase noise

is given by:

$$\frac{2}{\pi B}\frac{1}{\left[1+\left(\frac{2(f-f_c)}{B}\right)^2\right]}. \tag{3.12}$$

This LO signal, when used in a down-conversion mixer on a receiver, will generate a baseband signal that is the result of a passband signal spectrum convolved with this LO signal with non-zero bandwidth. Thus, the frequency components of the baseband signal will now be blended with the distortion products of the LO. This is specially harmful in OFDM signals since these are very sensitive to spectral spreading as it introduces phase errors on all its sub-carriers as well as ICI among them.

I&Q Imbalances

As seen in section 3.3.1, a zero-IF receiver presents a solution that down-converts the RF carrier signal directly to baseband DC. This is done by mixing the signal with the LO and the LO shifted 90°, originating an amplitude (I) and phase (Q) signal respectively. These however, can show some imbalances due to imperfect matching of both branches. This is known as I/Q imbalance and is one of the main problems in homodyne receivers.

In a given system with the received signal identical to the transmitted signal, as:

$$y(t) = Re\{x(t)e^{j2\pi f_c t}\} = x_I(t)cos(2\pi f_c t) - x_Q(t)sin(2\pi f_c t), \tag{3.13}$$

and with the transmitted signal as:

$$x(t) = x_I(t) + jx_Q(t), \tag{3.14}$$

the gain error is $20log\frac{1+\alpha}{1-\alpha}$ dB and the phase error as ϕ, the IQ imbalances can be modeled as:

$$\begin{aligned} &2(1+\alpha)cos(2\pi f_c t - \phi/2) \\ &-2(1-\alpha)sin(2\pi f_c t + \phi/2) \end{aligned} \tag{3.15}$$

By multiplying the passband signal to the two LO signals and passing through two lowpass filters,the demodulated baseband signals can be written as

$$\begin{aligned} \tilde{x}_I(t) &= (1+\alpha)\left[x_I(t)cos\left(\frac{\phi}{2}\right) - x_Q(t)sin\left(\frac{\phi}{2}\right)\right] \\ \tilde{x}_Q(t) &= (1-\alpha)\left[x_Q(t)cos\left(\frac{\phi}{2}\right) - x_I(t)sin\left(\frac{\phi}{2}\right)\right] \end{aligned} \tag{3.16}$$

From the previous equation it can be retrieved that IQ imbalance causes interference between I and Q signals. In figure 3.8, examples for imbalances in gain and phase are presented. In the frequency domain, the previous equation can be rewritten as:

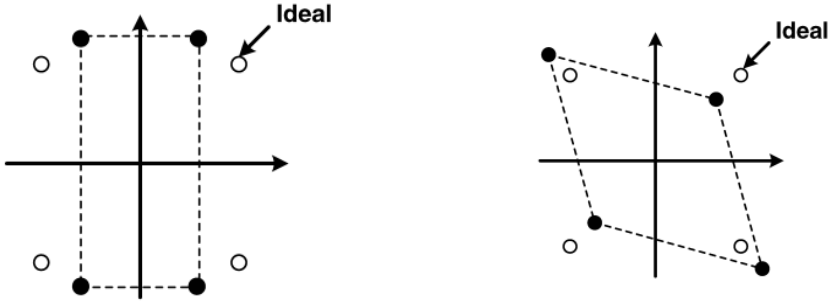
$$\begin{aligned}\tilde{x}(t) &= \tilde{x}_I(t) + j\tilde{x}_Q(t) \\ &= \left[cos\left(\frac{\phi}{2}\right) + j\alpha sin\left(\frac{\phi}{2}\right)\right]x(t) + \left[\alpha cos\left(\frac{\phi}{2}\right) + jsin\left(\frac{\phi}{2}\right)\right]x^*(t) \\ &= Ax(t) + Bx^*(t),\end{aligned} \tag{3.17}$$

where * denotes complex conjugate. For an OFDM system, the baseband signal is composed of k sub-carriers. As such, in the frequency domain an OFDM signal IQ Imbalances can be summed as: subcarrier

$$\left((X_{k,I} + jX_{k,Q})e^{j2\pi k f_s t}\right)^* = (X_{k,I} - jX_{k,Q})e^{-j2\pi k f_s t} = X_k^* e^{j2\pi(-k)f_s t} \tag{3.18}$$

As such, the received baseband OFDM affected by IQ imbalances is given by

$$\tilde{X}_k = AX_k + BX_{-k}^* \tag{3.19}$$



(a) (b)

Figure 3.8: IQ imbalances on QPSK received signal, with gain error (a) and phase error (b), from [45].

In sum, IQ imbalances on an OFDM signal introduce ICI due to the mirror sub-carrier and as such OFDM signals can be very susceptible to the IQ imbalance effect. To reduce this effect, when designing the front-end a special care must be given to the matching of the two branches or a compensation must be implemented on the baseband receiver.

3.3.3 Overall system performance fundamentals

SNR vs Eb/No

While E_b/No is usually confused with Signal-to-Noise Ratio (SNR), this relation translates a normalized SNR value per bit [48]. This translates to:

$$E_b = \frac{S}{R_b} \tag{3.20}$$

where R_b is the bit rate in bits/sec, E_b is the bit energy in Joules/bit and S is the total signal power in Watts.

From this, by inserting the noise factor, it is obtained the following:

$$\begin{aligned} \frac{E_b}{No} &= \frac{S}{R_b * No} \\ \Leftrightarrow \frac{S}{N} &= \frac{R_b * E_b}{No * B} \\ \Leftrightarrow SNR &= \frac{R_b * E_b}{No * B} \end{aligned} \tag{3.21}$$

where is seen that SNR is dependent on both E_b/No and the signal bandwidth. As such, by increasing the data rate, the SNR will increase but this will be achieved at the expense of increased noise factor (due to InterSymbol Interference (ISI), since more bits are packed closer and sent through the channel).

Thus, to improve signal quality, a compromise between SNR and R_b must be achieved for each given receiver.

EVM vs BER requirements

For the evaluation of the received signal quality, two main Quality of Service (QoS) metrics are used when using digital modulations: Error Vector Magnitude (EVM) and Bit Error Rate (BER).

EVM measures the quality of the modulation and the error performance of a com-

plex wireless system. This provides a method to evaluate the impairments that affect the signal reliability by measuring the symbol distortion in regards to the transmitted symbol. EVM is usually employed in multi-symbol modulations,such as QPSK and M-QAM. In figure 3.9, a representation of the error vector measurement is given.

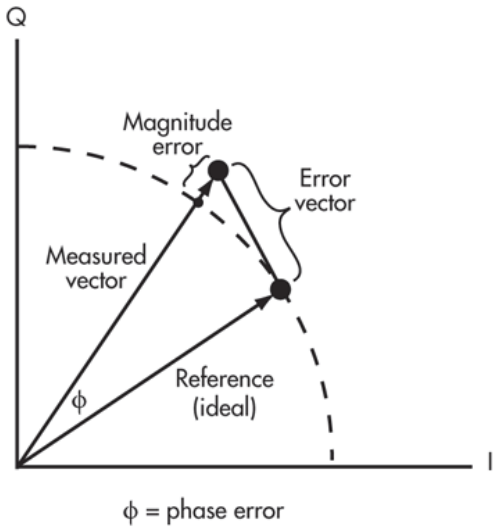


Figure 3.9: Error vector measurement, from [49].

This metric represents the ratio of the average error vector power (P_{error}) to the average ideal reference power (P_{ref}) can be represented in either decibel or percentage and is expressed as:

$$\begin{aligned} EVM[dB] &= 10log\left(\frac{P_{error}}{P_{ref}}\right) \\ EVM[\%] &= \sqrt{\left(\frac{P_{error}}{P_{ref}}\right)} \times 100 \end{aligned} \tag{3.22}$$

BER, on the other hand, provides a concrete evaluation of the performance by attributing the percentage of bit errors for a given number of transmitted bits. This metric is employed for any type of modulation.

Chapter 4

RF system characterisation

In this section, the OFDM-based system is introduced and characterised, from measurements of both performance and impairments on baseband and RF stages. Moreover, two types of RF front-ends are tested and compared in performance. In figure 4.1, an overall system block diagram is shown, with the different evaluated components.

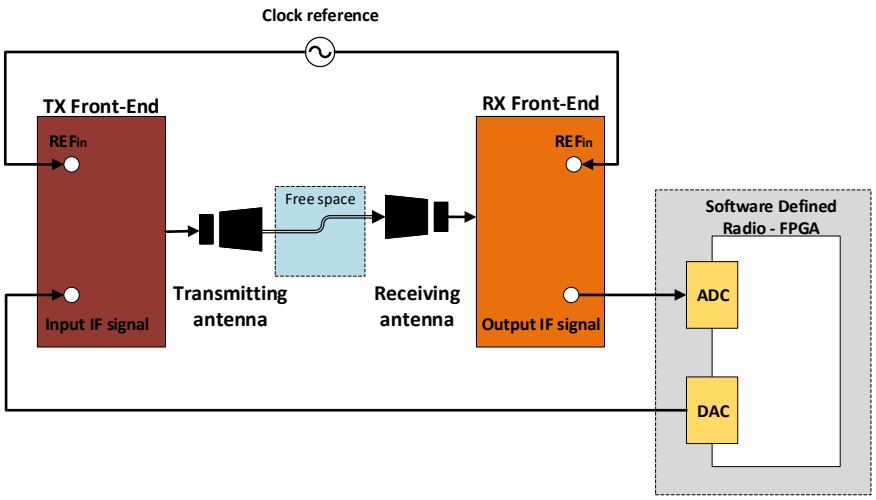


Figure 4.1: Overall system block diagram

4.1 Summary of main features

As seen in section 2.1, the 5G will require systems capable of providing high bursts of data at low latency. As such, in this work an OFDM FPGA-SDR system, based on the work in [50], is characterized and presented. The FPGA selected was the VC707 from Xilinx [51], due to being the most powerful board available on the market, i.e., the one

with the most resource blocks. Since the FPGA works on a digital domain, converters between both digital to analogue states and vice-versa are required. The DAC and ADC selected were the FMC 230 and FMC 126, respectively. These were chosen due to being the only one's in the market that met this work's requirements in sampling rate, binary resolution and compatibility with the VC707 FPGA. Both converters are configured for a sampling frequency of 1250 MHz, with filters at the DAC output in order to eliminate signal replicas above 520 MHz.

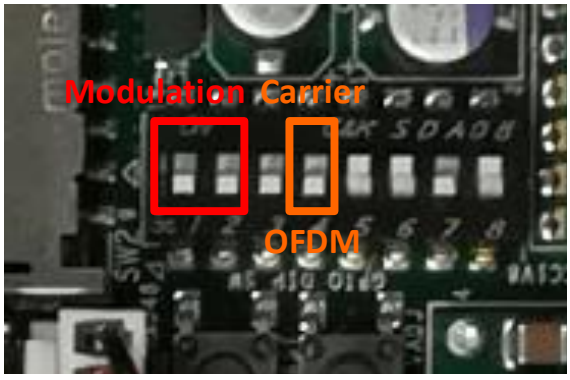
Figure 4.2: Considered SDR developed system for wideband signals.

The Multi-Gigabit system here proposed, shown in figure 4.2, was based on the Physical (PHY) layer of the LTE standard [21] and consists of an OFDM modulation with 4-, 16-, 64-, 256-QAM. In order to perform over-the-air transmission, algorithms for timing and frame synchronization, channel and CFO estimation and compensation are considered. Moreover, to distinguish the synchronisation sequence and reduce possible synchronisation errors at the expense of a higher PAPR, this presents a 15 dB amplitude from the remaining data carriers. The SDR system specifications are presented in table 4.1.

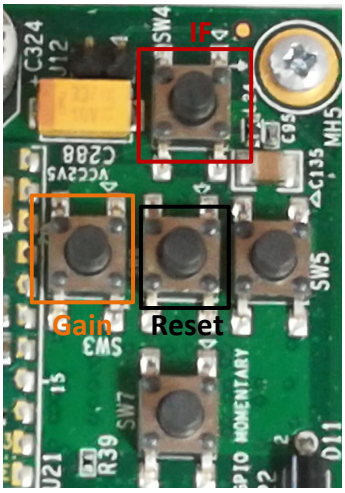
Table 4.1: Considered SDR system specifications.

Feature	Value
Processing BW	1.25 GHz
Transmission BW	150 MHz
ADC/DAC sampling rate	1.25 GSamples/s
Modulation	OFDM 4/16/64/256-QAM
Max spectral eff.	8 bits/s/Hz/user
IF freq.	DC-612 MHz
User configuration	Single
Antenna configuration	SISO
Number of DAC/ADC channels	2/3
Resolution of DAC/ADC	14/10 bits

The VC707 board has both a dual-in-line package (DIP) switch and push-buttons that allow for the manual configuration of the system, from IF selection, to modulation, digital gain or selection between OFDM and carrier signal, as seen in figure 4.3. This gives a fast and interactive way to perform a real-time evaluation for the different scenarios, without requiring the system to be reprogrammed.



(a)



(b)

Figure 4.3: VC707 board: (a) DIP switch and (b) pushbuttons.

The SDR back-to-back (B2B) performance was assessed in order to provide a baseline for the following measurements. As such, this measurement was carried on by connecting the DAC0 to the ADC0 channel (I Channel), DAC1 to the ADC1 channel

(Q Channel) and with both connections simultaneously. Each measurement was conducted for four IF f_c: 0 (baseband), 2 (f_c @ 156.25 MHz), 2 (f_c @ 312.5 MHz) and 2 (f_c @ 468.75 MHz). The obtained results are shown in the following table, with the best case received signal constellations for all four modulations presented in figure 4.4.

Table 4.2: System Performance B2B with various channel configurations for various IF values

IF	**EVM I channel**		**EVM Q channel**		**EVM IQ channel**	
	[%]	**[dB]**	**[%]**	**[dB]**	**[%]**	**[dB]**
0	-	-	-	-	320.76	11.17
2	0.85	-41.29	**0.77**	**-42.21**	13.10	-17.31
4	**0.84**	**-41.51**	0.78	-42.10	0.87	-41.23
6	0.97	-41.22	0.90	-40.86	**0.72**	**-42.75**

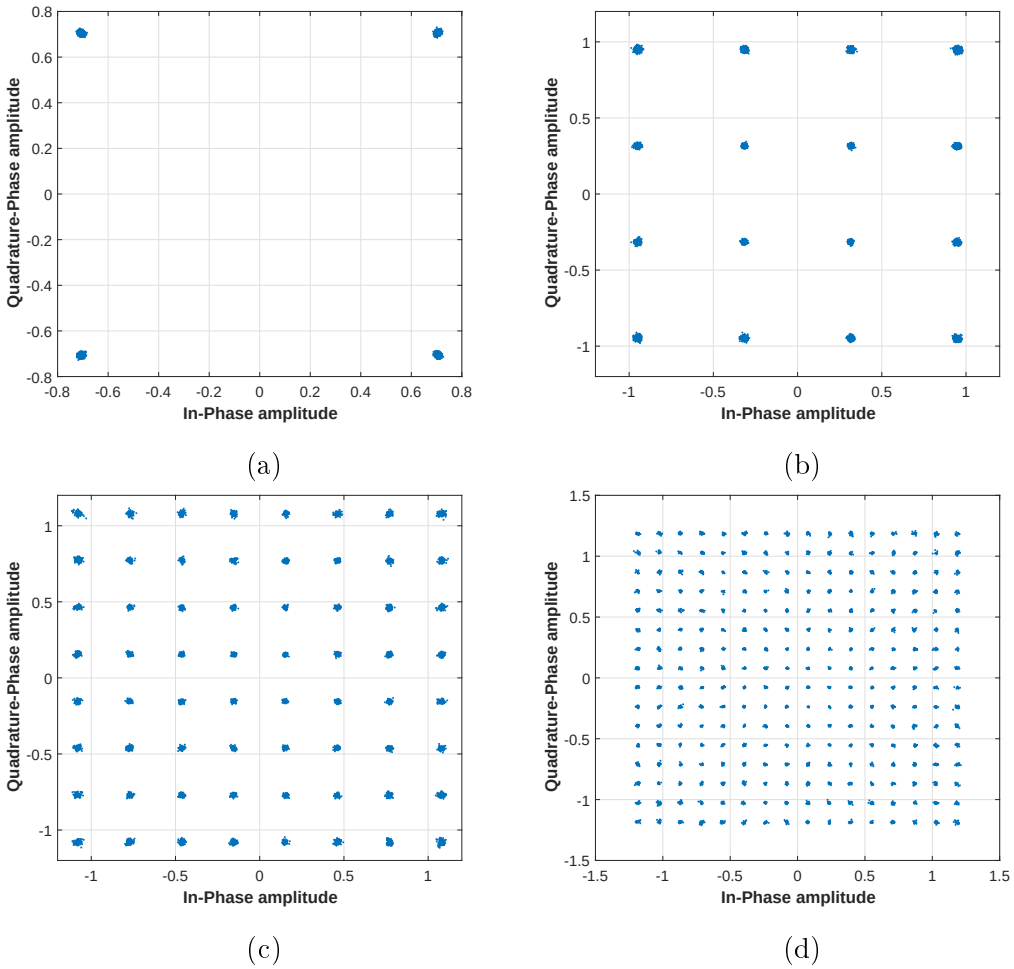


Figure 4.4: Received B2B signals with: (a) QPSK, (b) 16QAM, (c) 64QAM and (d) 256QAM.

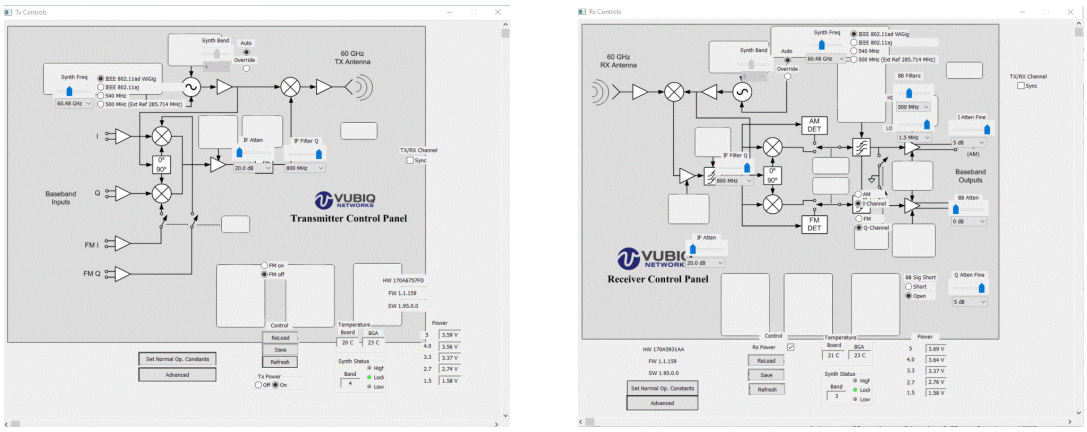
Throughout the evaluation of this work, EVM is used as the main QoS metric. In order to infer if its value presents a good signal quality for a given modulation, from the work in [50], the following table was constructed with the minimum QoS that allow the signal to be decoded effectively.

Table 4.3: System QoS metrics requirements

Modulation	**EVM [dB]**	**BER**
QPSK	-9	10^{-2}
16 QAM	-15	10^{-2}
64 QAM	-25	10^{-2}
256 QAM	-32	10^{-2}

In regards to the RF Front-end, two different approaches were considered, the VUBIQ PEM009 and the Instituto de Telecomunicações (IT) Front-end.

The VUBIQ PEM009 is a commercially available 60 GHz TX-RX Front-end development system which can be configured by the user through a Universal Serial Bus (USB) interface connected to a host Personal Computer (PC) [52]. This configuration is performed on a Guide User Interface (GUI) (figure 4.5), supplied by the manufacturer, that enables the user to choose multiple parameters, such as RF f_c, baseband filter bandwidth, amplifier attenuation or channel spacing. While both TX and RX boards possess a built-in clock reference, an outsourced solution was developed to study the performance of the Front-ends on a shared reference clock source configuration. In the following figure, both TX and RX GUI's are shown.



(a) (b)

Figure 4.5: VUBIQ PEM009 GUI for TX (a) and RX (b) boards.

The TX board, figure 4.6, is responsible for the up-conversion of both IQ differential baseband signals. As such, the first step is to up-convert the signal in an IQ mixer with a LO frequency f_{LO1}. This mixer translates and combines both IQ signals at Baseband Frequency (f_{BB}) into an IF signal (f_{IF}). Then, the IF signal is amplified and filtered by a baseband filter to eliminate image signals from the previous mixing stage. The amplification gain may be tuned through an attenuator (IF_{Att}) through the GUI to prevent PA saturation. Subsequently, the IF signal is modulated to the transmission f_c through the second mixing stage, with LO at f_{LO2}. All the reference oscillator frequencies (f_{LO1},f_{LO2} and the Voltage Controlled Oscillator (VCO) frequency f_{VCO}) are generated by the inherent synthesizer, that is referenced by the external differential reference clock to lock the VCO's Phase Lock Loop (PLL). As such, a relation between the different frequencies can be achieved and is shown as:

$$\begin{cases} f_{LO1} = f_{VCO} \times \frac{1}{2} \\ f_{LO2} = 3 \times f_{VCO} \\ f_{VCO} = f_c \times \frac{2}{7} \\ f_{RF} = f_c + f_{BB} \\ f_{IF} = f_{LO1} + f_{BB} \end{cases} \tag{4.1}$$

where f_{RF} is the transmission frequency.

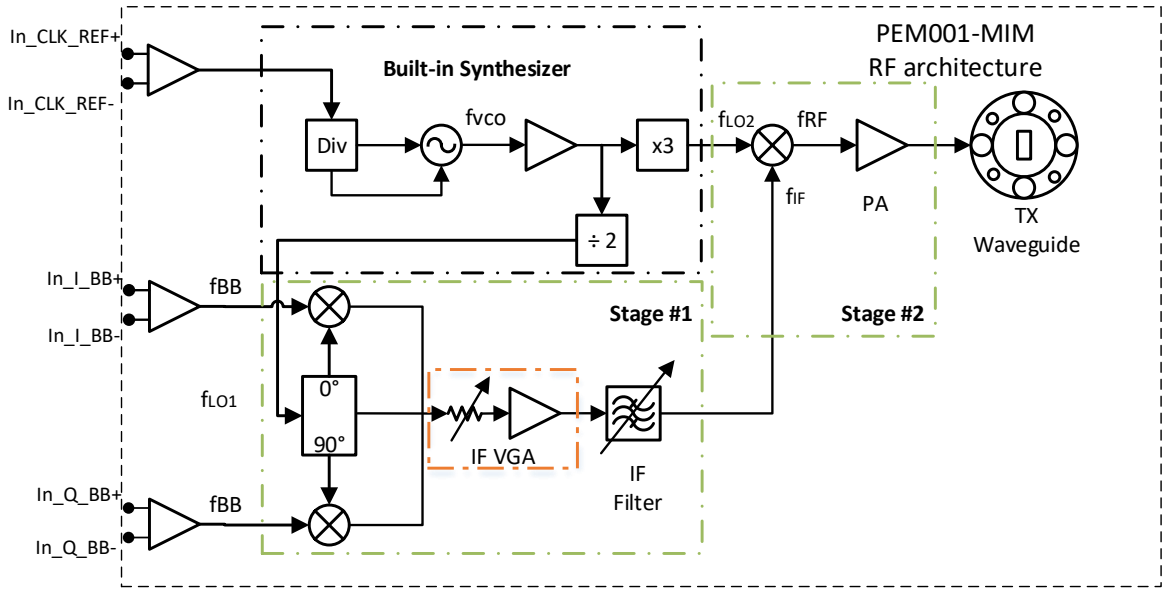


Figure 4.6: VUBIQ PEM009 transmitter two-step superheterodyne up-conversion architecture, based on [52].

On the RX Board, figure 4.7, the inverse process is performed, also on two stages. The received mmWave signal is first amplified by a Low Noise Amplifier (LNA). Then, a

frequency down-conversion is performed to move the RF signal to the IF band. Following this procedure, various amplification and filtering stages are performed to suppress image signals and adjust the IF signal to the optimal IQ demodulation. Finally, the down-conversion to baseband is performed by an IQ mixer with the resulting signal passing through another amplification and filtering stage to suppress signal replicas, images and prevent signal aliasing from the previous down-conversion processes.

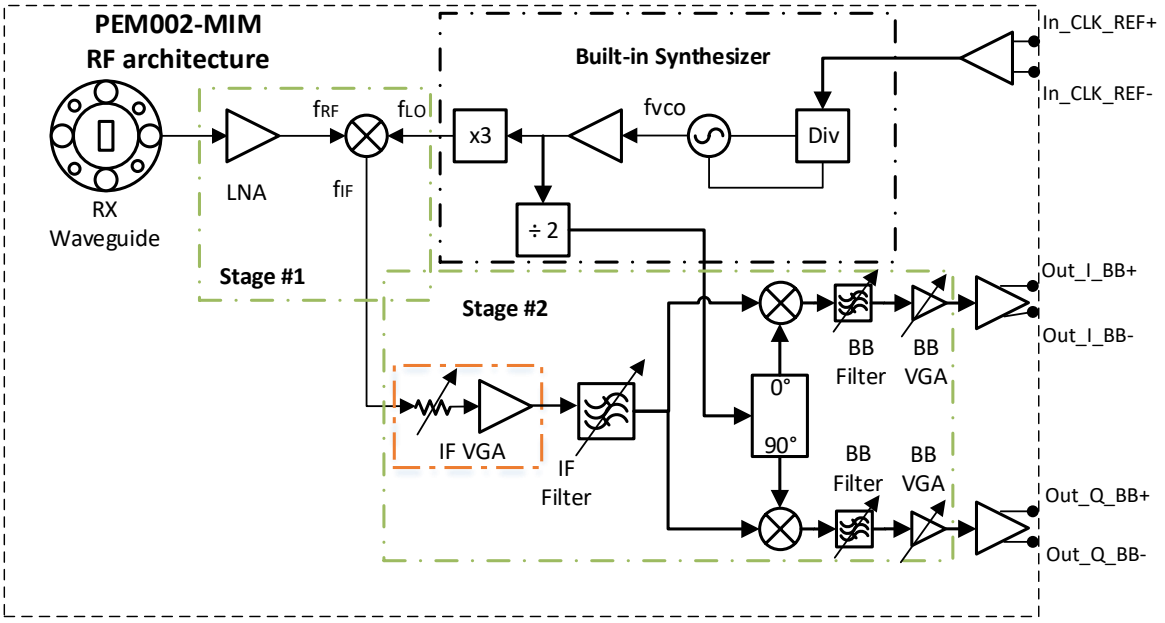


Figure 4.7: VUBIQ PEM009 receiver two-step superheterodyne down-conversion architecture, based on [52].

Besides this commercial solution, a customizable system was also tested for this work. The IT Front-end is a fully custom 60 GHz Front-end composed of several HXI analogue components connectorized. This system has been previously used for a 60 GHz radar solution [53] and for the measurement of 60 GHz signal propagation in vegetation [54]. This custom solution is designed to provide a multi-Gigabit/s radio in-the-loop solution at mmWave without CFO. The IT TX, figure 4.8, has a homodyne mixer with a 15 GHz LO. This brings the baseband signal to 15 GHz of f_c which is then passed through a 4X multiplier to lead the output RF signal to 60 GHz. A 10 MHz signal at the input provides the reference signal to the 15 GHz PLL. This transmitter does not employ a PA at its output in order to prevent possible PA saturation and non-linearities induced in the signal.

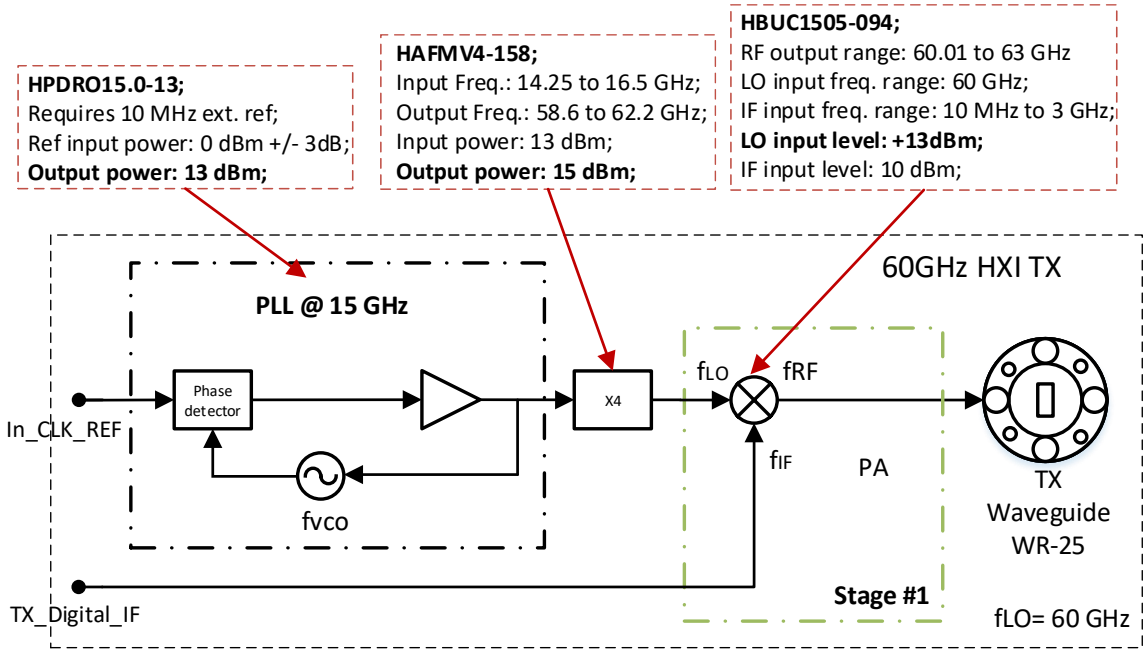


Figure 4.8: IT homodyne up-conversion transmitter.

On the IT RX, a heterodyne down-conversion mixer is employed. As with the TX PLL, the RX PLLs have a reference input signal of 10 MHz. On the first mixing stage, the 60 GHz received signal is passed through an LNA to amplify the received signal. This is then down-converted to a 6 GHz IF stage by the first mixing stage with a LO of 54 GHz, generated by a 13.5 GHz PLL and a 4x multiplier. On the second mixing stage, a 6 GHz PLL acts as the mixing stage LO and brings the IF signal to baseband.

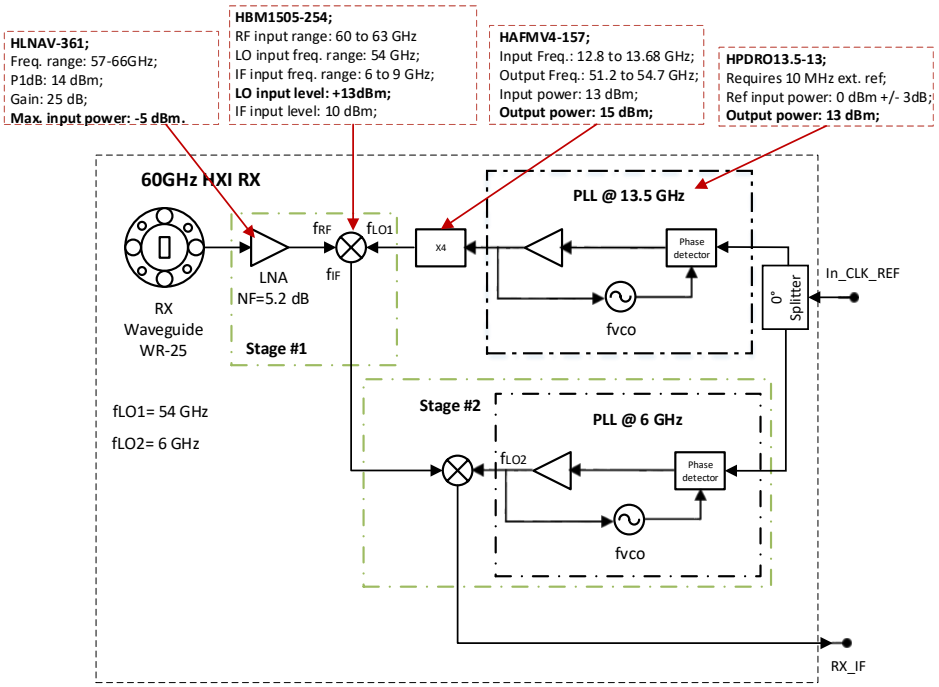


Figure 4.9: IT two-step heterodyne down-conversion receiver.

In the following figure, both RF Front-end solutions are presented.

(a) (b)

Figure 4.10: RF Front-end solutions: (a) VUBIQ PEM009 and (b) IT.

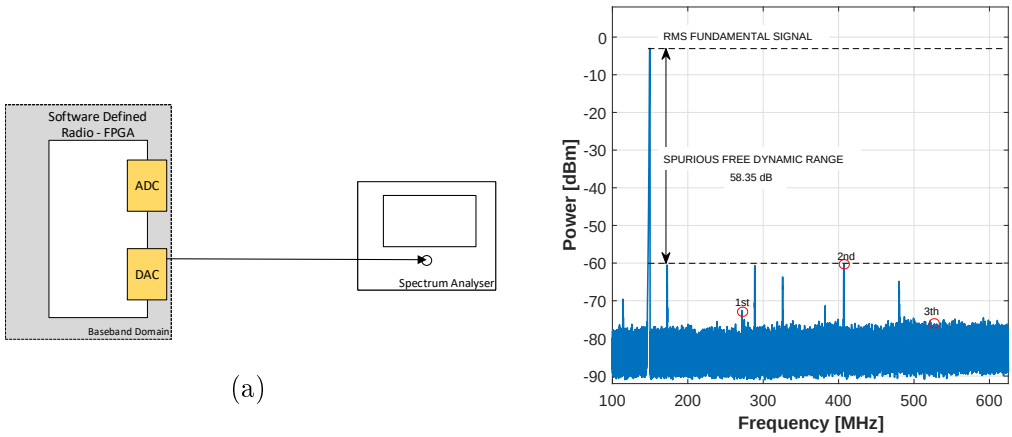
Furthermore, a hybrid solution with VUBIQ and IT front-ends at different ends of the transmission system was also employed and evaluated.

4.2 Baseband

In this section, the baseband impairments are assessed and characterized. This characterization will be performed on the DAC and ADC, clock reference signals and AGC.

4.2.1 DAC

As stated in section 3.2.2, DAC's SFDR gives its dynamic range value. To measure this, a carrier DAC output signal was connected to a spectrum analyser and output to a PC for post-processing. The SFDR was obtained by measuring the difference, in dB, between the RMS signal and the first harmonic. It was also obtained, in post-processing, the values for DAC's SINAD and ENOB for different IF carrier frequencies in order to establish DAC's frequency response. Figure 4.11 presents the measurement block diagram and the SA input signal with f_c at 134.3 MHz.



(a)

(b)

Figure 4.11: DAC SFDR: (a) measurement block diagram and (b) output signal at 134.3 MHz.

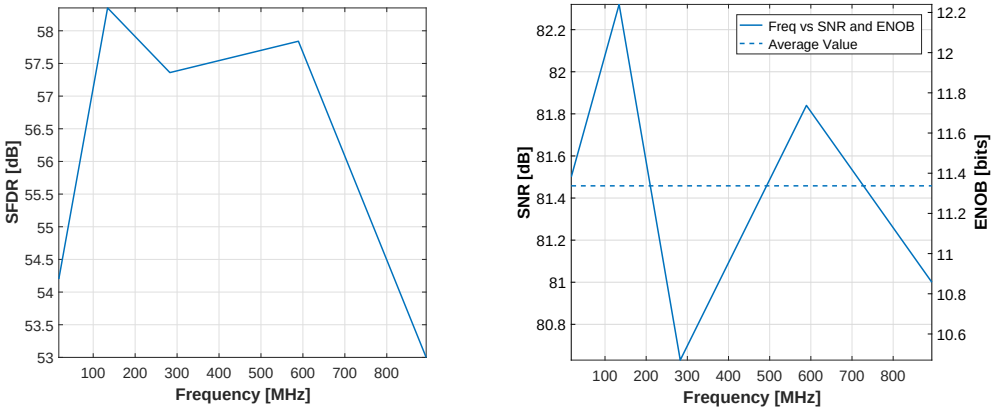
In figure 4.11b, it is possible to verify spurious noise that is not centred at any harmonic frequency. This may come from DAC's internal noise and is not considered for the SFDR measurement. As stated before, in order to establish the frequency response of the DAC, the input signal was changed through multiple IF values in carrier signal mode, with the SFDR, ENOB and SNR values measured for each case. These results are presented in the following table.

Table 4.4: SFDR measurement on SDR DAC.

Freq. [MHz]	**Carrier Power [dBm]**	**Noise Floor [dBm]**	**SFDR [dB]**	**SNR [dB]**	**SINAD [dB]**	**ENOB [bits]**
18	-3.5	-85*	54.2	81.5	75.48	12.25
134.3	-2.68	-85*	58.35	82.32	64.77	10.47
282.8	-4.37	-85*	57.36	80.63	68.75	11.13
589.3	-3.16	-85*	57.84	81.84	71.03	11.51
893.9	-4	-85*	53	81	68.05	11.01

* Value measured by the average value in the noise floor, with 3 kHz Resolution Bandwidth.

These results have been summarized in the following figures.



(a) (b)

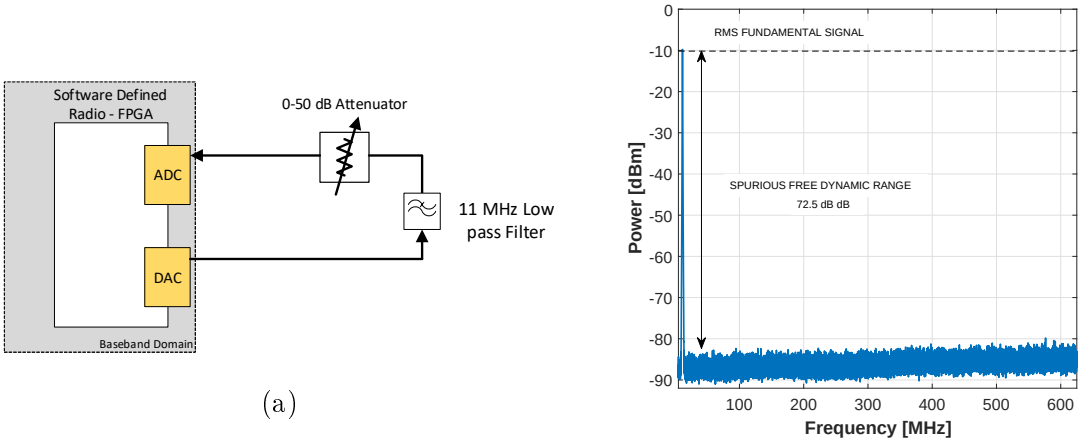
Figure 4.12: Obtained results for tone frequency response: (a) SFDR and (b) SNR & ENOB.

From the previous figure, it is seen that the SFDR is relatively stable throughout the carrier signal frequency, with a maximum deviation of 5 dB between carrier frequencies. Moreover, from the analysis of both SFDR and SNR & ENOB curves, it is possible to conclude that the DAC performs well throughout its frequency range and is therefore not a restriction for the overall system performance.

4.2.2 ADC

For the ADC, SFDR measurements were also conducted. This was done by introducing at the ADC input a 9 MHz carrier signal. This signal, generated by the DAC, was

filtered by a 11 MHz low-pass filter to eliminate harmonics and internal noise that may interfere in this measurement. The 9 MHz filtered signal, presented in figure 4.13, was first connected to a SA and its value of SFDR was measured. This will work as a baseline to evaluate the performance degradation due to the ADC.



(a) (b)

Figure 4.13: ADC SFDR: (a) measurement block diagram and (b) 9 MHz input signal.

The DAC output filtered signal presented a SFDR value of 72.5 dB, with almost no harmonics. This signal was fed to the ADC and its performance was evaluated according to figure 4.14. This figure shows the degradation in the 9 MHz signal resulting from the ADC.

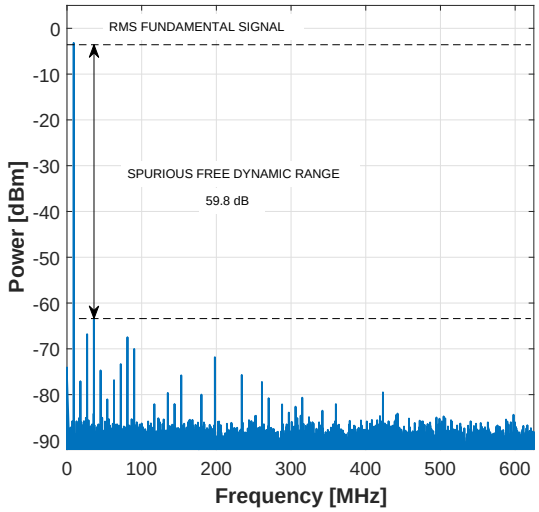


Figure 4.14: SFDR at ADC output with 9 MHz carrier signal.

The ADC induced a performance degradation of 12.7 dB which means that the ADC has a dynamic range of 59.8 dB. A 0-50 dB variable attenuator was also placed between the low-pass filter and the ADC input to evaluate the ADC performance for

signals with input power between -10 and -60 dBm. The resulting SNR and ENOB was then measured for this input range, as shown in the following figure.

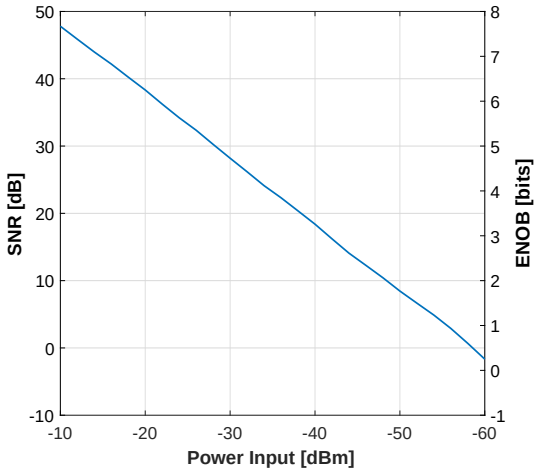
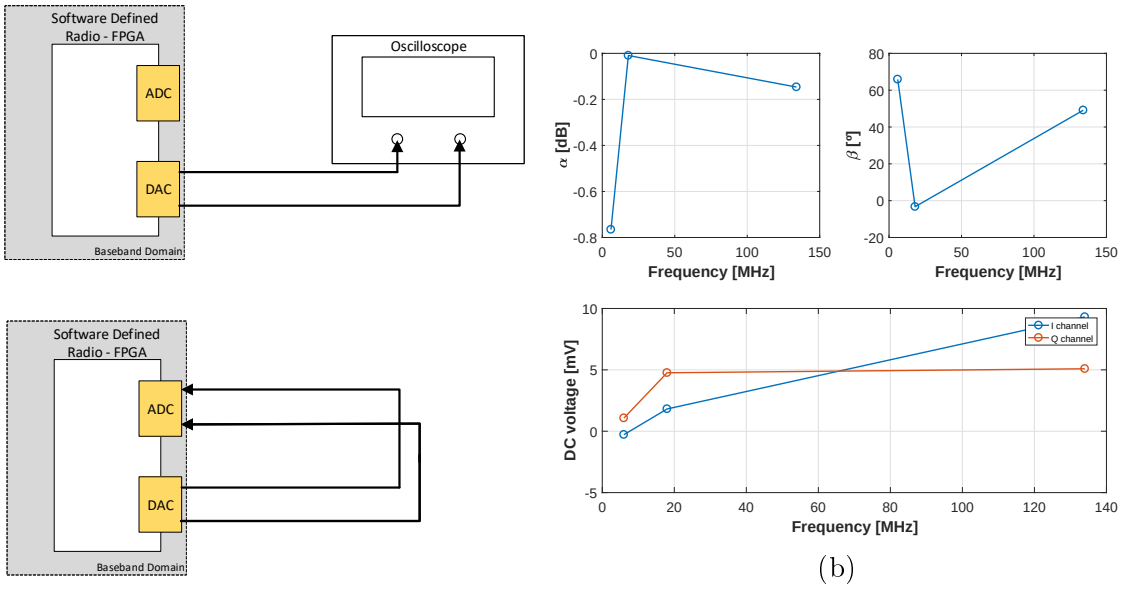


Figure 4.15: ADC SNR & ENOB vs Power Input.

From the previous figure it is possible to conclude that, as expected, the higher the input power, the higher the obtained SNR and ENOB value. Furthermore, for instance, from table 4.3, it is possible to see that to decode a signal employing 16QAM an EVM value of -15 dB is required. By rule of thumb, EVM is inverse to SNR, with a -1 dB of EVM corresponding to 1 dB of SNR. As such, from the previous figure is possible to see that to decode a 16QAM signal, the ADC input signal power must be higher than -44 dBm. A detailed characterisation of the required input power is shown in section 4.3.1.

The next step was to measure the ADC IQ imbalances. For this end, the IQ signals from the DAC were input on an oscilloscope and their phase offset was adjusted to be as close to 90° as possible. These were then introduced on the ADC and their phase (β) and amplitude offset (α) were measured. The measurement procedure and results are shown in figure 4.16.



(a) (b)

Figure 4.16: ADC IQ imbalances: (a) measurement block diagram and (b) gain, phase and voltage offset over its frequency range.

The previous results show were measured for three different input carrier signal frequencies (6,18,134 MHz) and show that for all considered frequencies, IQ imbalances do occur. However, this is less predominant on lower frequency signals. Furthermore, for a input signal of 18 MHz, no amplitude or phase imbalances occurred.

4.2.3 Phase noise characterization of the clock sources

In the baseband signal, three LOs were considered for the clock reference signal for the two RF Front-ends considered. These were a: a crystal oscilattor M6300 [55] for the VUBIQ Front-end, the PRS10M rubidium oscillator [56] to be used in the custom IT solution and as a reference for the ADC and DAC and a synthesizer evaluation board to be used in a hybrid IT-VUBIQ solution.

M6300

The M6300 crystal oscillator is a differential output oscillator which outputs a square wave signal for reference in the PEM009 boards. Although a reference board is commercially available, in order to reduce the overall cost and allow to replicate this board

for independent clock signals, a Printed Circuit Board (PCB) had been developed with the M6300 crystal soldered. This crystal was chosen due to its higher stability in comparison with the internal reference. For example, while the internal reference presented a stability of 25 ppm, this oscillator is capable of providing a stability value of 0.5 ppm., where ppm stands for parts per million and it translates the signal deviation, in Hz, every million seconds, that is, the higher this value, worst clock signal performance is achieved. For example, in a 60 GHz signal, this difference may result in a CFO of 1.5 MHz and therefore make it impossible to decode. In figure 4.17 this reference board is shown.

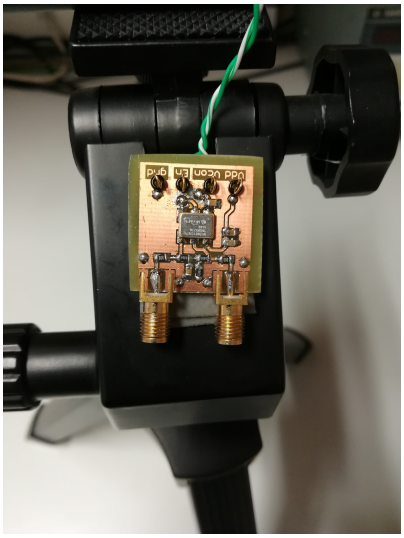


Figure 4.17: M6300 crystal.

To infer the clock reference signal performance, a phase noise measurement was performed. This was done by connecting the differential output signal of the reference board to a 180° combiner splitter which then was connected to a SA. In the following table, the phase noise measurement of this board is shown for the square wave's f_c.

Table 4.5: Phase Noise on M6300 crystal reference.

Frequency Offset [Hz]	**Phase Noise [dBc/Hz]**
10	-62
100	-78.5
1000	-80
10000	-99
100000	-118
1000000	-124

Rubidium

The rubidium clock, shown in figure 4.18, was allocated for three scenarios: as a reference clock for the PLLs of both up and down-converters, reference signal to the DAC and ADC and as reference signal for a synthesizer. This clocks outputs a 10 MHz signal with a frequency stability of 0.5 ppb (parts per billion). Therefore, this reference signal presents a high enough stability for all given cases.

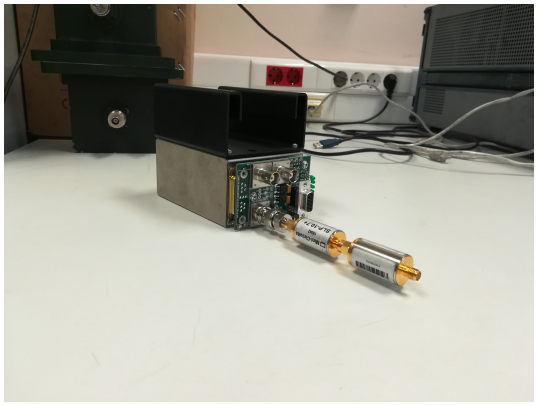


Figure 4.18: Rubidium Oscillator.

As with the M6300, to evaluate the rubidium oscillator performance, its phase noise was measured. For this end, a low-pass filter with cut frequency of 11 MHz was placed at the PRS10M to reduce harmonic distortion. This was then connected to the SA and its phase noise values retrieved and shown in the table 4.6.

Table 4.6: Phase Noise on rubidium.

Frequency Offset [Hz]	**Phase Noise [dBc/Hz]**
10	-78
100	-80
1000	-81
10000	-100
100000	-122
1000000	-128

ADF4350 Synthesizer

To provide a LO signal for the Hybrid solution, a synthesizer evaluation board from Analog Devices, the EVAL-ADF4350 [57] (fig. 4.19), was used. This synthesizer contains an internal 25 MHz reference signal. However, to improve the reference signal stability, a 50Ω resistor was placed to enable an outsourced reference signal, in this case the 10 MHz rubidium clock signal.

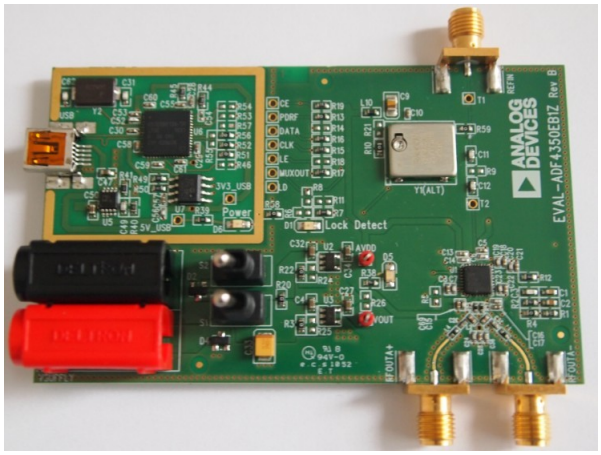


Figure 4.19: ADF4350 synthesizer evaluation board.

The differential output of this board was then combined with a 180° splitter and connected to a SA for a phase noise measurement, with its result shown in the following table.

Table 4.7: Phase Noise on Synthesizer@308.571 MHz.

Frequency Offset [Hz]	**Phase Noise [dBc/Hz]**
10	-78.4
100	-80
1000	-83
10000	-98.6
100000	-115.7
1000000	-119.4

Clock references' comparison

In the following figure, a performance comparison between the different oscillator's phase noise is shown.

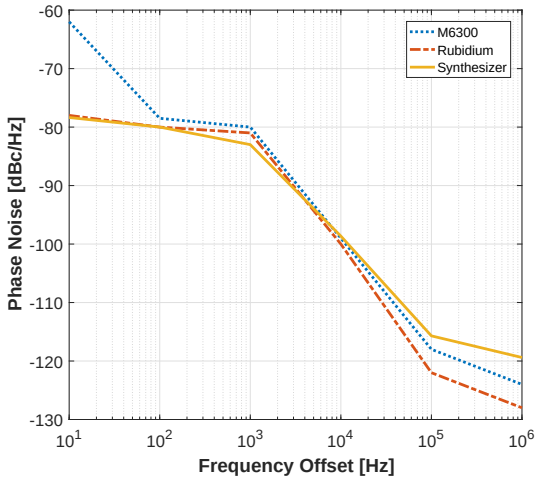


Figure 4.20: Clock sources measured phase noise.

From the previous figure it is possible to infer that the rubidium clock source presents the best overall performance, as expected.The synthesizer performs similarly to the rubidium due to being referenced by it, with the M6300 performing the worst, although showing similar results for frequencies higher than 1000 Hz from f_c.

4.2.4 Automatic Gain Control

In order to maximize the system operating range and guarantee the maximum input power at the ADC, an AGC device was constructed. This device uses two MAX2090 analogue VGAs [58] and a HMC1030, a dual-port power detector [59]. The use of a two port system is related to the expandability of this system to a 2x2 MIMO solution in the future or to be used in a serial configuration. In order to accommodate this device, a case was constructed whose dimensions are shown in A.2. Furthermore, this device required four types of voltages for both power supply and to provide a reference signal to both VGAs. As such, a PCB was developed, powered by a single 12V power supply which powers four DC-DC converters, that connect to the various devices. The reference signals are connected to a potentiometer to adjust the output power to the desired value. The schematic of this PCB can be found on A.1 and the final system is presented in the following figure.

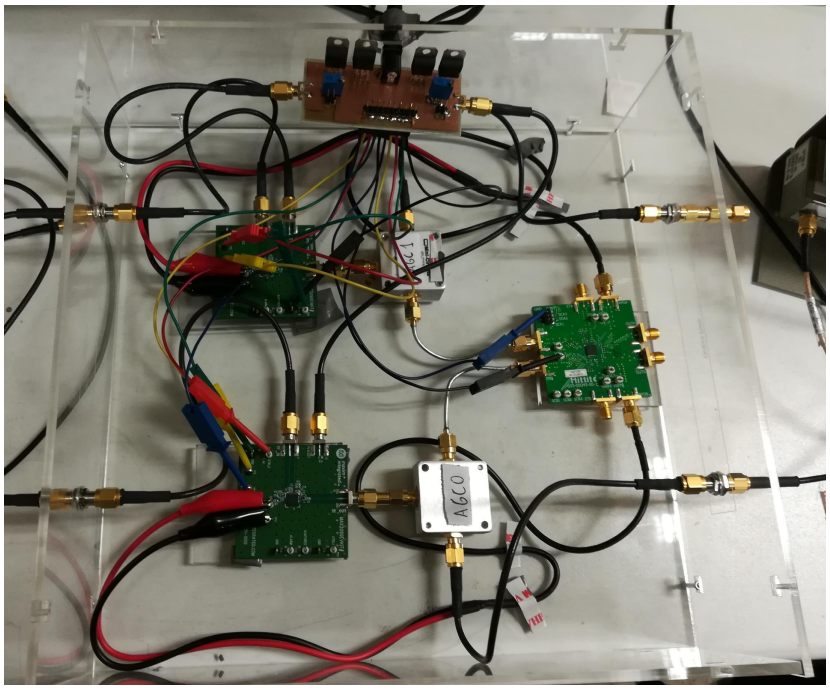


Figure 4.21: Developed AGC device.

This system was then evaluated with both AGCs set to the same reference voltage and for -10 dBm output. Following the setup shown in 4.22, the AGCs performance was evaluated for both its output vs input power and its EVM stabilization for a B2B configuration with an OFDM signal. To this end, an analogue variable attenuator was placed between the DAC output and the AGC input that varied the AGC input signal power between -20 and -48 dBm..

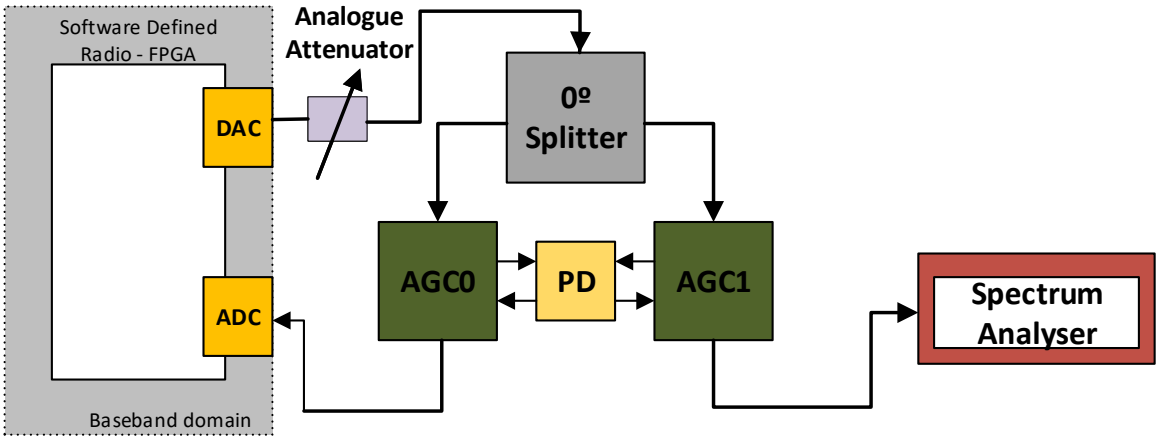
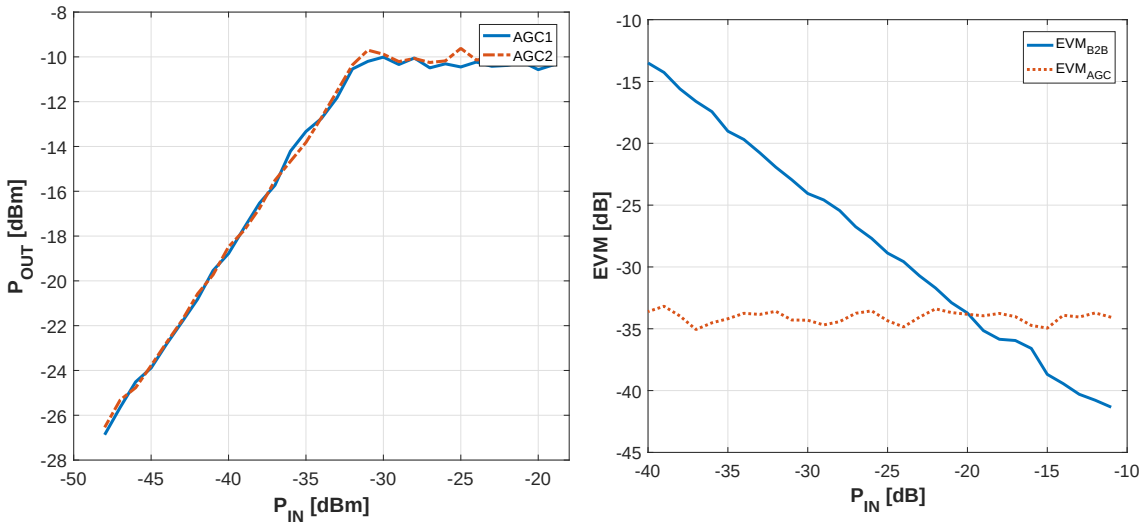


Figure 4.22: AGC measurement setup.

The performance results are shown in figure 4.23 which shows that the output power has stabilized at -10 dBm for around 13 dBs, which is in accordance with the

VGA amplifier maximum gain of 25 dB. Furthermore, as the input power decreases, the output signal decreases linearly with this value. As for the output EVM, this value remains stable throughout the input range. While the input signal EVM decreases as the input power decreases, thanks to the introduction of the AGC, this QoS metric remains stable.



(a) (b)

Figure 4.23: AGC performance results for: (a) input power and (b) EVM.

4.3 RF front-end

Following the evaluation of the baseband components of the SDR, the two RF front-ends were tested. For the performance evaluation and measurements, a QPSK signal was used.

4.3.1 VUBIQ

The VUBIQ PEM009 was evaluated inside an anechoic chamber to diminish possible multipath effect. Furthermore, the TX and RX boards were placed 64.5 cm apart at LOS, with a 25 dBi horn antenna on TX and a 0 dBi antenna on the RX to prevent saturation on the receiver's LNA. Both TX and RX amplifier attenuators were set on their GUI to 20 dB, thus settling both amplifiers to their minimum gain. The connection diagram is shown in the following figure.

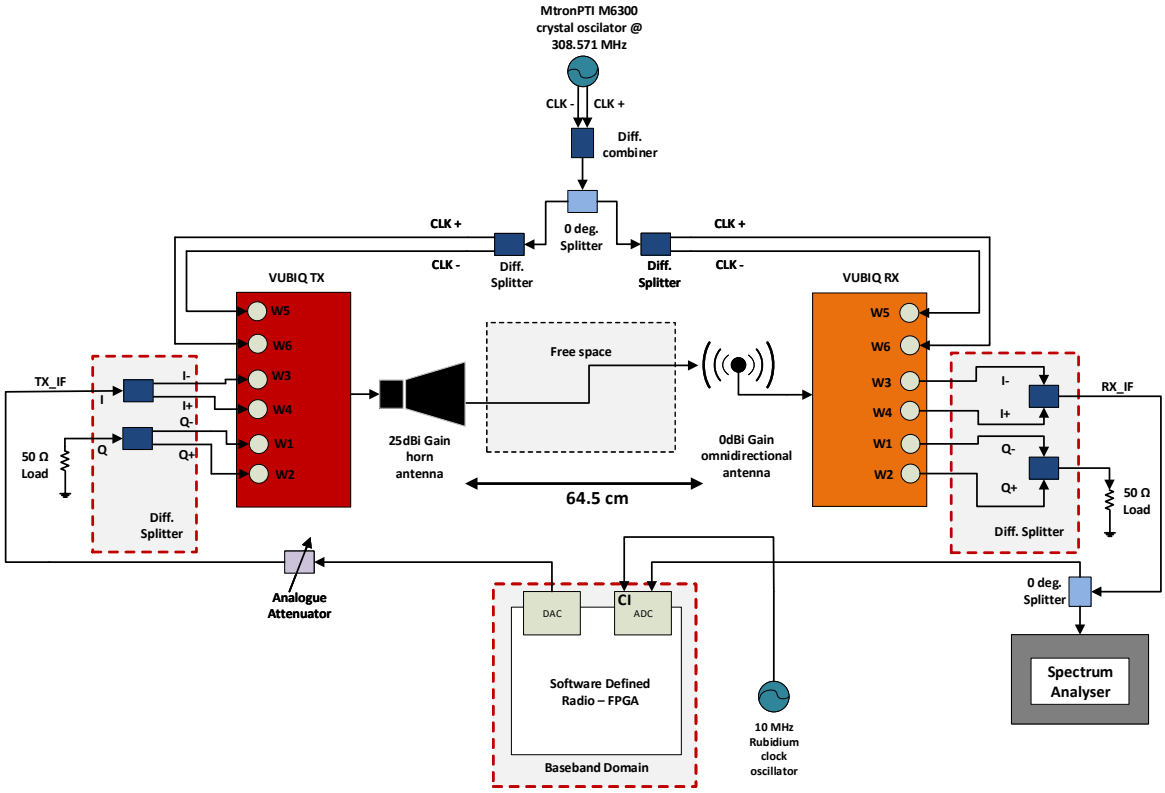


Figure 4.24: VUBIQ connections diagram.

To evaluate the signal performance and prevent saturation, an analogue attenuator is placed at the output of the DAC, varying between 0, 5 and 10 dB. Moreover, the input signal was changed between its different digital gain values (0 to 7) and IF f_c (IF2, IF4, IF6).

Phase noise

The first measurement performed was of the received signal phase noise. In order to perform this measurement, a carrier signal was transmitted and its performance was evaluated through the SA. The first configuration tested was with a shared reference clock, to avoid possible CFO between each board- In the following table, the obtained phase noise results are shown.

Table 4.8: Phase noise on VUBIQ with shared reference clock.

Frequency Offset [Hz]	**Phase Noise [dBc/Hz]**
10	-3.03
100	-26.07
1000	-35.98
10000	-39.31
100000	-47.64
1000000	-59.27

The RX carrier is shown in the following figure, which as expected does not present any CFO.

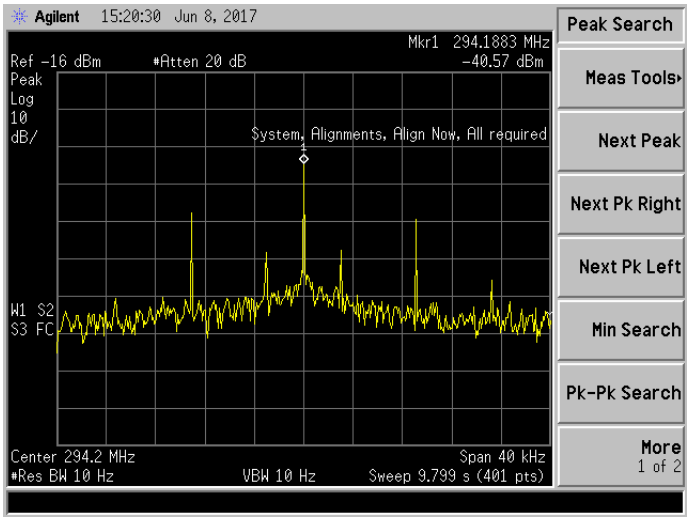


Figure 4.25: RX carrier signal on VUBIQ with shared reference clock.

In a real world scenario, both TX and RX do not present a shared reference clock. As such, an independent reference source was also tested and evaluated. Its phase noise results are shown in the following table.

Table 4.9: Phase noise on VUBIQ with independent reference clock.

Frequency Offset [Hz]	**Phase Noise [dBc/Hz]**
10	-11.76
100	-29.75
1000	-42.04
2250	-2.09
10000	-45.76
100000	-52.64
1000000	-69.88

As can be seen, a peak at 2250 Hz offset was obtained which shows that CFO has occurred between TX-RX. This can also be seen in the following figure, where two peak signals are present in the received signal.

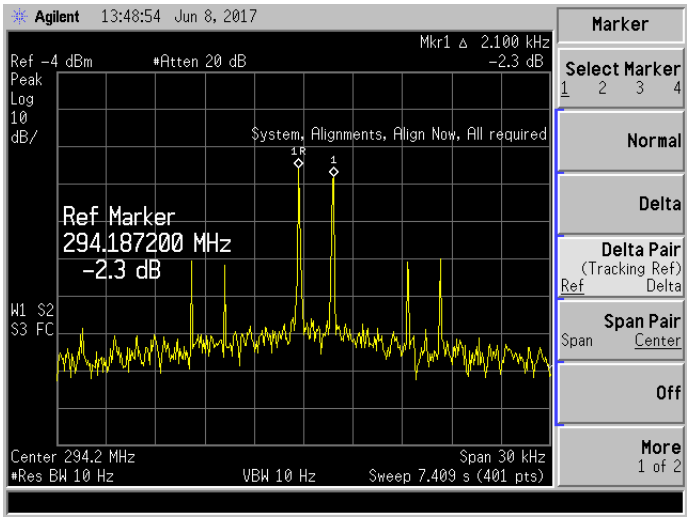


Figure 4.26: RX carrier signal on VUBIQ with independent reference clock.

A summary and comparison between both clock configurations is presented in figure 4.27. It is possible to conclude from this figure that although the independent clock source shows a slightly better performance than the shared clock configuration, it also presents CFO that prevents the signal from being correctly decoded by the baseband system.

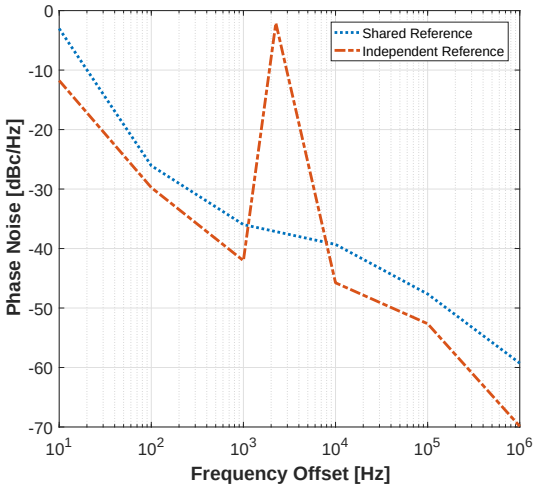


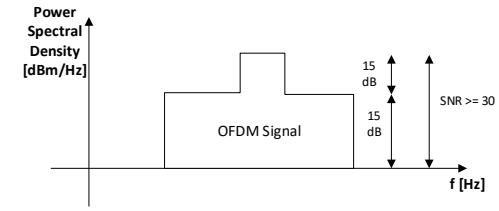
Figure 4.27: Phase noise comparison between shared and independent clock configurations on VUBIQ front-end.

System noise floor

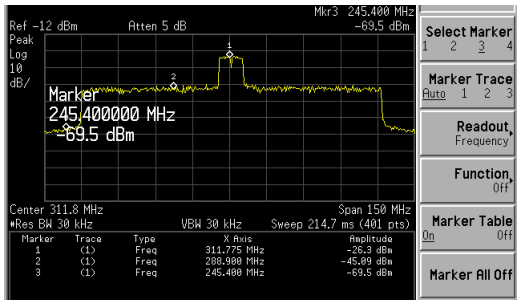
As stated in section 4.1, the system's OFDM signal presents a synchronisation sequence with 15 dB higher power than the remaining symbols. This results in the need for higher input power to properly decode the information for a given modulation. In section 4.2.2, it was stated that in order to decode a 16 QAM signal, an ADC input power of -44 dBm was required, for the given 15 dB of SNR. However, due to the increased amplitude of the synchronisation sequence, to properly decode the 16QAM signal, it is now required 30 dB of SNR, as shown in figure 4.28a. As such, the input ADC power must now be of -28 dBm.

Thus, to evaluate the VUBIQ output power and determine if this is in accordance with the required output signal power, the system noise floor was measured and the overall OFDM signal power determined. This value was first measured on the spectrum analyser for 10 kHz of span and 10 Hz of resolution bandwidth with the transmitter turned off. The obtained value was of -96 dBm, which results in a system noise floor of -136 dBm, as shown in the following equations.

$$\begin{aligned} No_{@10kHz} &= -96dBm \\ \Rightarrow N_o &= -96 - 40 \\ \Leftrightarrow N_o &= -136dBm \end{aligned} \tag{4.2}$$



(a)



(b)

Figure 4.28: OFDM signal: (a) required SNR and (b) received B2B signal.

In regards to the OFDM symbol, the system noise floor was given by calculating the power in the signal bandwidth, as such:

$$\begin{aligned} 156MHz &= 82dB/Hz \\ No/156MHz &= -136 + 82 \\ \Leftrightarrow No/156MHz &= -54dBm \end{aligned} \tag{4.3}$$

As such, in order to obtain a SNR of 30 dB, the input power on the ADC must be, at minimum, -24 dBm.

4.3.2 IT RF front-end

In the evaluation of IT Front-end, this was also set inside an anechoic chamber to prevent multipath effects. Its TX and RX were equipped with a 25 dBi horn antenna, to compensate for the fact that the TX device does not have a PA. These were distanced 74.5 cm apart at LOS with a 16 dB amplifier on the received baseband signal to improve the RX signal power. To provide the 10 MHz PLL reference signal, the rubidium clock source was employed due to their high signal stability, as seen in section 4.2.3.

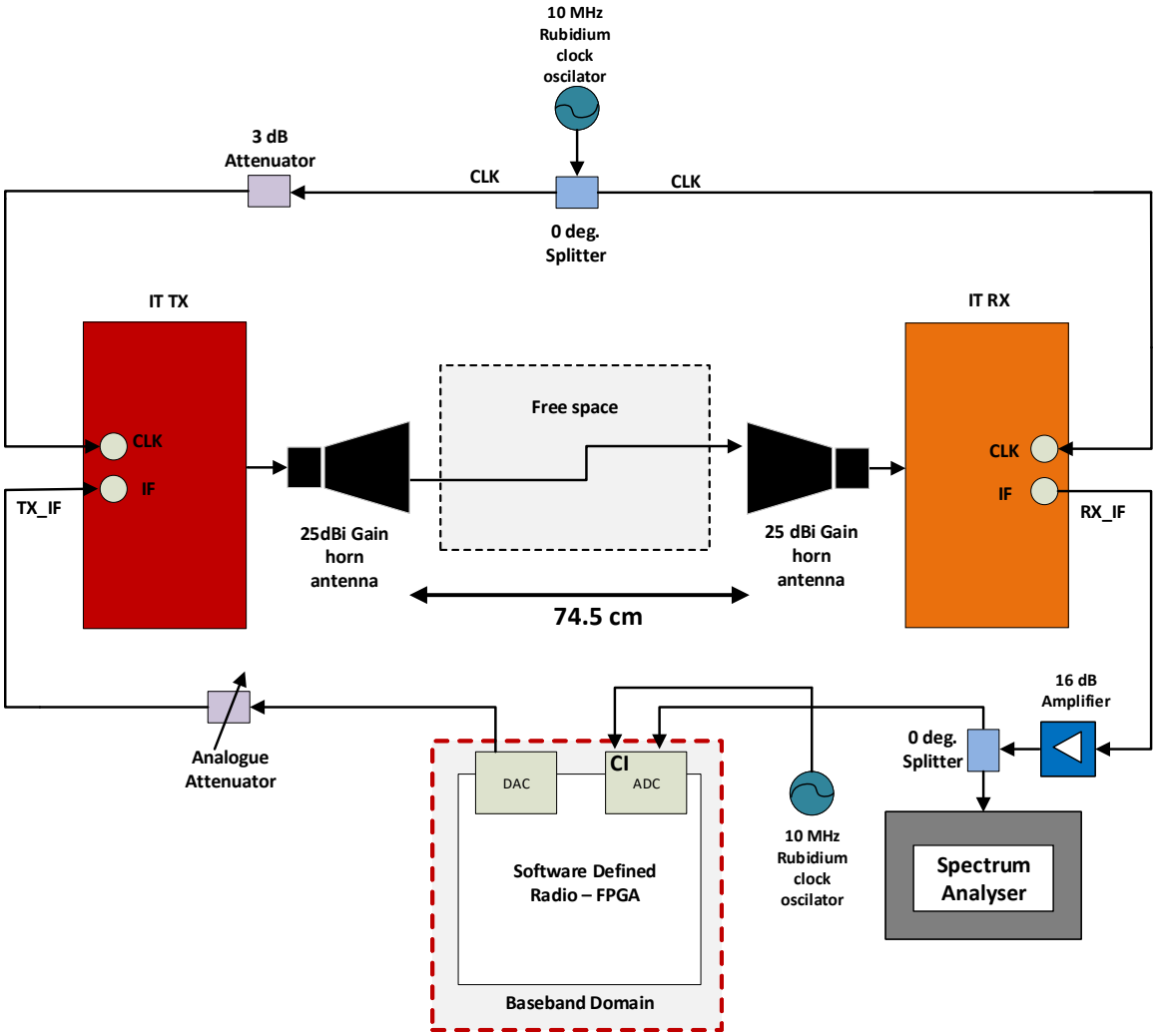


Figure 4.29: IT connections diagram.

Phase noise

To infer the RX signal quality, the first step in the IT front-end evaluation was to measure its phase noise on both shared and independent clock sources. In the shared clock configuration, one rubidium clock was used to provide both reference signals. On the RX side, the RX signal is divided into two equal signals by a 0° splitter to provide reference for the two PLLs employed. As such, to guarantee the same input power on both TX and RX PLLs, a 3 dB attenuator is inserted on the TX's reference input (power loss on the 0° splitter). Furthermore, a 5 dB attenuator was introduced at the rubidium output to prevent input signal saturation on the PLLs. These results are presented in table 4.10, with the received carrier signal shown in figure 4.30.

Table 4.10: Phase noise on IT with shared reference clock.

Frequency Offset [Hz]	**Phase Noise [dBc/Hz]**
10	-43.09
100	-43.28
1000	-66.97
10000	-79.36
100000	-84.56
1000000	-86.56

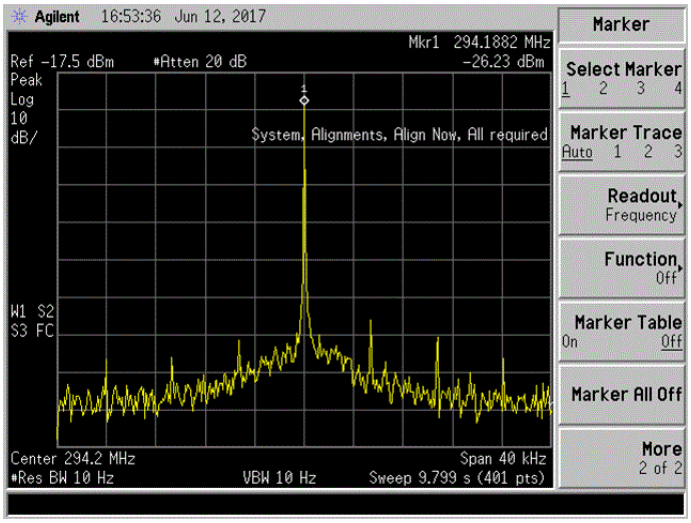


Figure 4.30: RX carrier signal on IT with shared reference clock.

Following this, two rubidium clock sources were used to provide independent references to both systems. Since the PLLs on both TX and RX require an input signal power between -3 and 3 dBm, a 3 dB attenuator was introduced on both sides, with the previous 3 dB TX attenuator replaced by a 6 dB one. These results are shown in table 4.11.

Table 4.11: Phase noise on IT with independent reference clock.

Frequency Offset [Hz]	**Phase Noise [dBc/Hz]**
10	-35.08
100	-47.68
1000	-72.01
10000	-85.40
100000	-88.20
1000000	-98.60

The received carrier signal is presented on the following figure where it is possible to see that no CFO has occurred, in contrast with the independent case on the VUBIQ front-end.

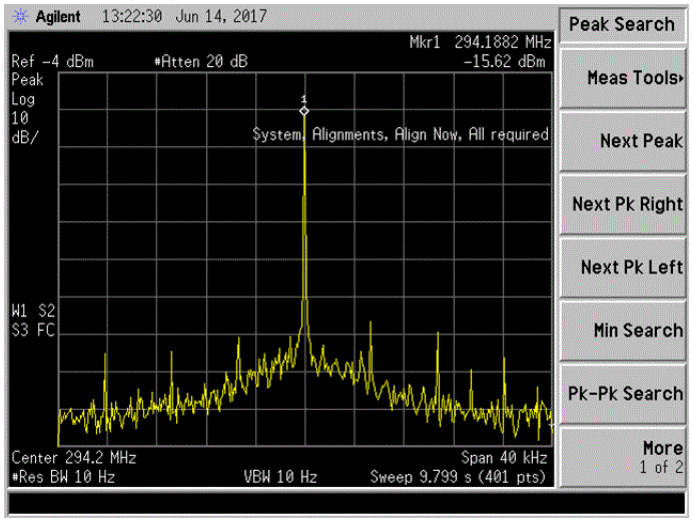


Figure 4.31: RX carrier signal on IT with independent reference clock.

Finally, a comparison between both clock configurations is presented on the following figure.

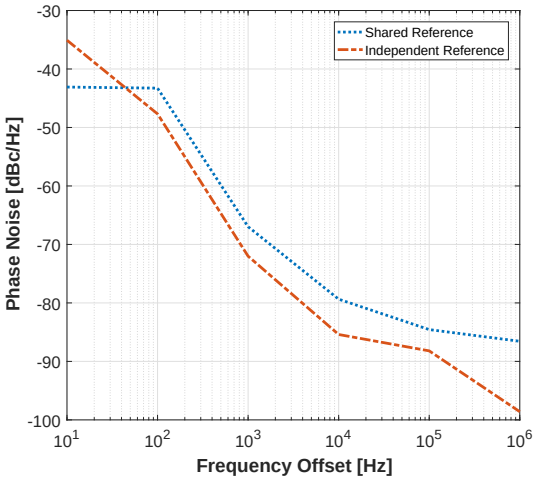


Figure 4.32: Phase noise comparison between shared and independent clock configurations on IT front-end.

4.3.3 Hybrid Configuration

To make use of both systems in a future MIMO system, a hybrid configuration was tested. Two approaches were considered for the use of both front-ends in a single system. These were an analogue approach with a CFO compensation conducted with a mixer on the RX side and an digital approach where the transmitted baseband IF signal was shifted to the desired frequency compensation, i.e. this signal digitally compensated for the analogue CFO.

Phase noise

To evaluate both approaches, a phase noise measurement was conducted on the SA. While various cases were conducted for these approaches, the phase noise measurements were performed for the best case scenarios, with 480 MHz CFO on the analogue approach (table 4.12) and 60 MHz CFO on the digital approach (table 4.12).

Table 4.12: Phase noise on analogue approach with VUBIQ TX and IT RX with 480 MHz CFO.

Frequency Offset [Hz]	**Phase Noise [dBc/Hz]**
10	-18.91
100	-42.08
1000	-54.14
10000	-59.28
100000	-69.14
1000000	-76.39

The RX carrier signal on the analogue approach is shown in the following figure, where it is possible to visualize that no apparent CFO has occurred, which may result in the RX signal to be properly decoded.

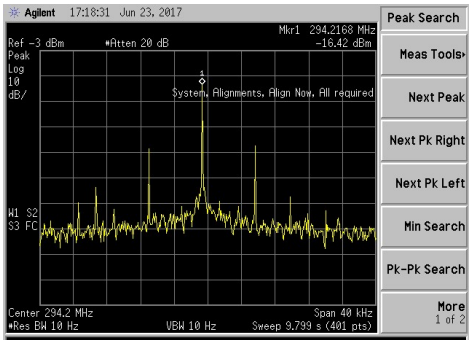


Figure 4.33: RX carrier signal on analogue approach with VUBIQ TX and IT RX with 480 MHz CFO.

The phase noise measurement values of the digital hybrid approach are shown in table 4.13, with the RX carrier signal presented in figure 4.34, where CFO and spurious signal are present in higher quantities and amplitude than in previous cases.

Table 4.13: Phase noise on digital approach with VUBIQ TX and HXI RX with 60 MHz CFO.

Frequency Offset [Hz]	**Phase Noise [dBc/Hz]**
10	-17.77
100	-27.69
1000	-47.23
10000	-60.31
100000	-72.76
1000000	-79.59

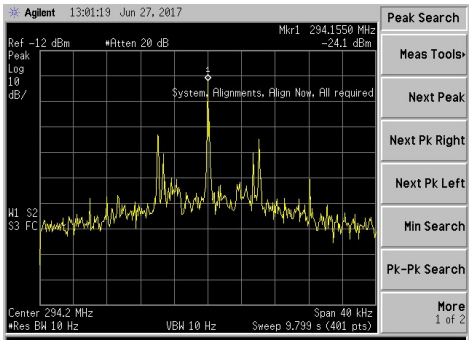


Figure 4.34: RX carrier signal on analogue approach with VUBIQ TX and HXI RX with 480 MHz CFO.

The comparison between both approaches is shown in figure 4.35, where it is possible to see that the analogue approach performs better than the digital one in terms of phase noise.

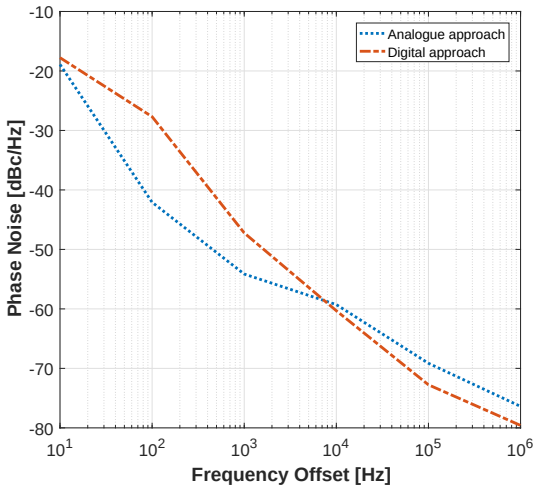


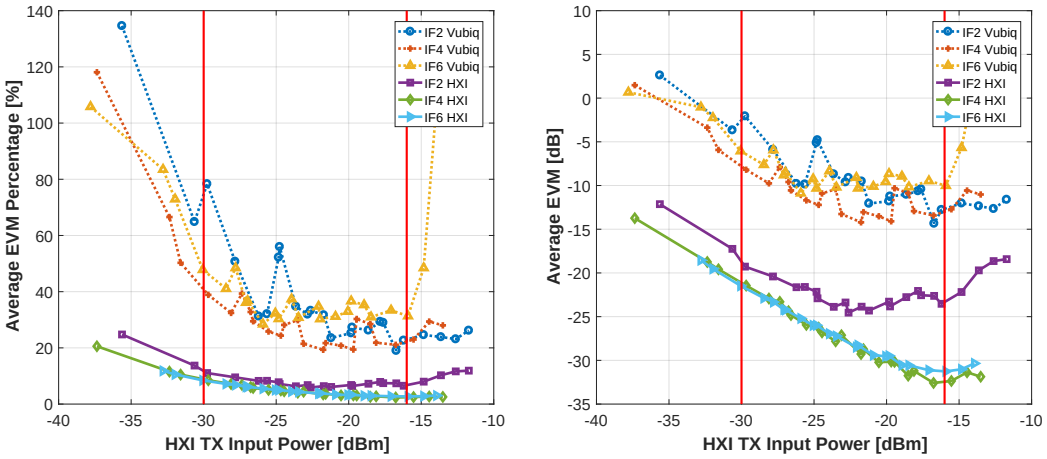
Figure 4.35: Phase noise comparison on hybrid configurations.

4.4 Overall system performance and constraints under AWGN channels

In this section, a comparison between the VUBIQ and IT technologies performance is presented. These will be performed on both shared and independent reference clock signals for a range of input signal power. The overall measurement results can be seen on appendix C, with a summary of these presented next.

4.4.1 System performance comparison on shared reference clock

The first measurement performed on both fron-ends was with a shared clock reference. These measurements were performed for all three baseband IFs, to determine which would perform best. In figure 4.36, a performance comparison between VUBIQ and IT front-ends with shared clock is shown where it is seen that the IT system presents improved performance than with the COTS VUBIQ solution.



(a) EVM Percentage.

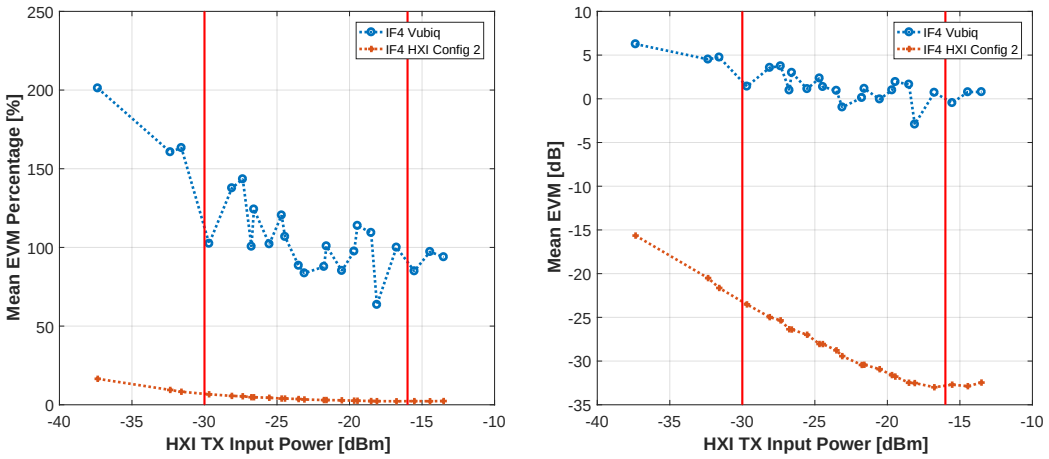
(b) EVM dB.

Figure 4.36: VUBIQ and IT performance comparison on shared clock reference.

The IT solution was able to achieve results better than -30 dB of EVM. This shows that this is able to decode a 256QAM signal which translates to a 1 Gbps data rate, in accordance with the 5G requirements presented in section 2.1. This measurement has also shown that the VUBIQ system, on its best case scenario, is only able to decode 16QAM signals, which results in being able to only transmit half the data rate of IT's front-end.

4.4.2 System performance comparison with independent reference clock

For the independent reference clock measurements, as seen in section 4.3.1, the VUBIQ system presents CFO when employing this configuration. As such, this system was only measured employing one IF configuration. Since in the shared clock configuration the IF4 performed best on the VUBIQ system, this was chosen for these measurements. As for the IT solution, all IF configurations were considered and measured. These results are shown in the following figure, with a comparison between the IF4 case for both systems.



(a) EVM Percentage.

(b) EVM dB.

Figure 4.37: VUBIQ and IT performance comparison on independent clock reference.

The VUBIQ system, due to its limitations in both performance and due to the CFO resulting from the independent clock signals, the receiver is not capable of being decoding data for any modulation. The IT front-end, on the other hand, performs similarly to the shared clock configuration, which shows that this system is capable of even performing best than the shared reference clock of the VUBIQ front-end.

4.4.3 Hybrid front-end

In order to maximize the return of both technologies for a MIMO configuration, the next phase was to use a hybrid configuration between both technologies. Two type of approaches were considered for these measurements:

- Type 1: VUBIQ TX and IT RX;
- Type 2: IT TX and VUBIQ RX.

The overall setup for both configurations is presented in figure 4.38.

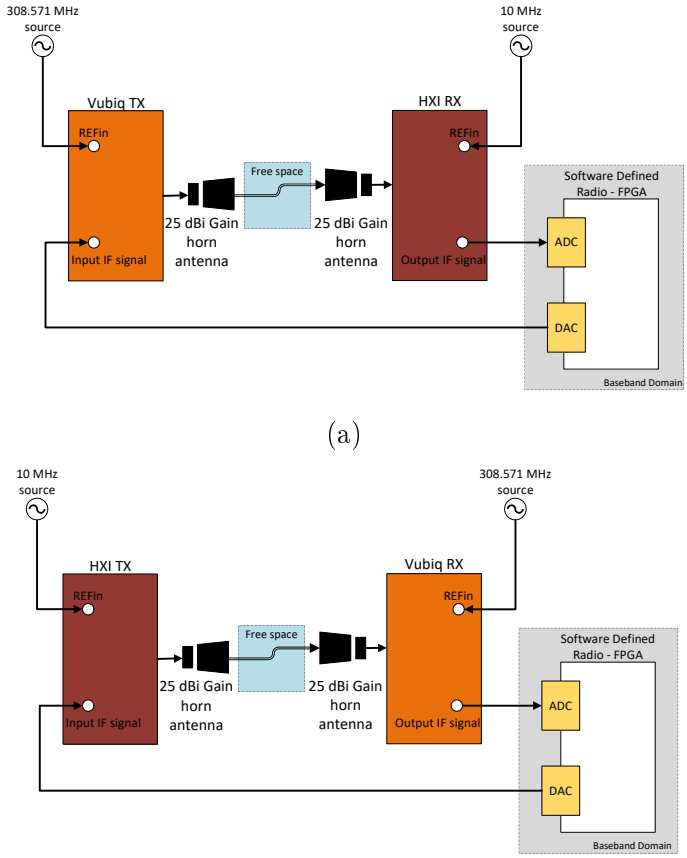


Figure 4.38: Hybrid setup configurations for: (a) type 1 and (b) type 2.

The problem with using a hybrid configuration is that the f_c for the VUBIQ and the IT are different. The IT has a single value for its f_c, at 60 GHz, while the VUBIQ has various values for f_c, ranging from: 58.86 GHz to 61.02 GHz, with none of these being 60 GHz. As such, different approaches were conceived to reduce the CFO between both technologies. These are split into two main approaches: an analogue approach and a digital approach.

Analogue Approach

The analogue approach makes use of the synthesizer mentioned in chapter 4.2.3. This synthesizer will be used as a LO for a mixer implemented on the received signal. In order to diminish the signal replicas due to the signal CFO and the insertion of a Mixer, four low-pass filters, with cut-off frequency of 550 MHz, were inserted in the baseband receiver side, as shown in figure 4.39.

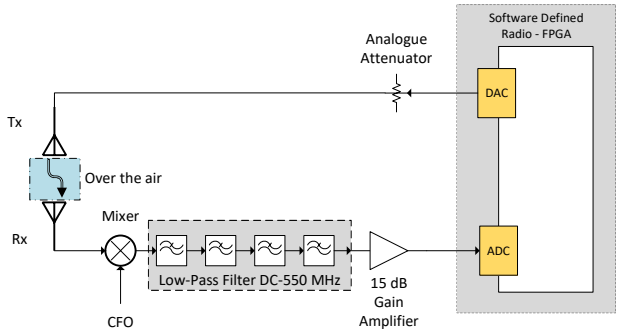
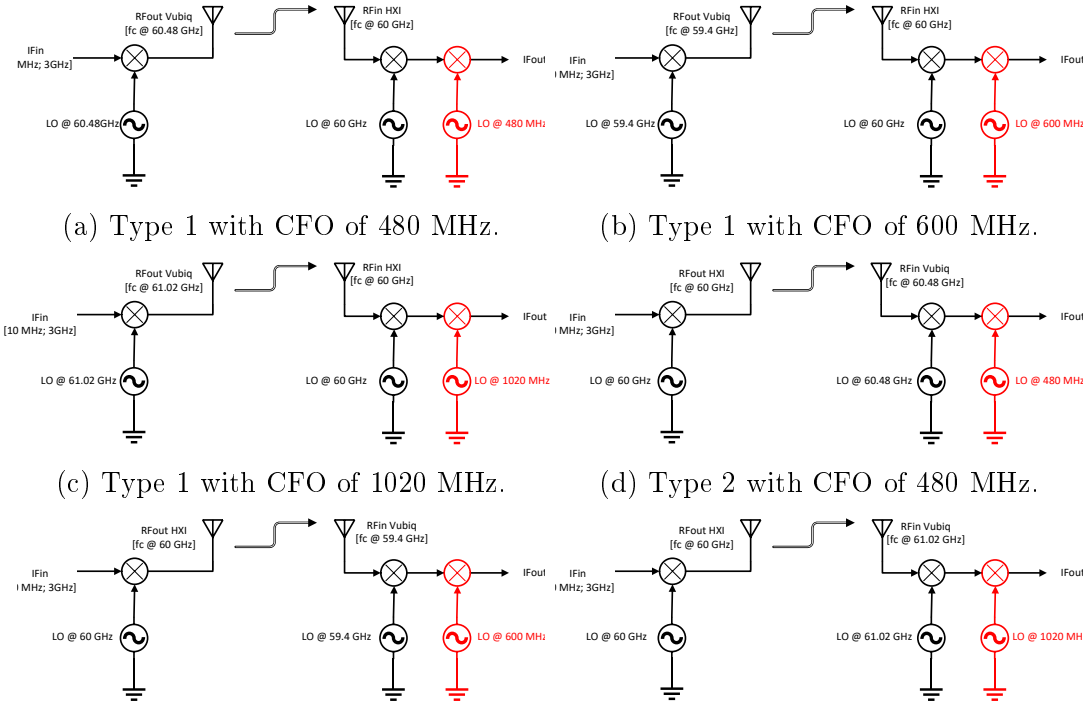


Figure 4.39: Analogue hybrid measurements CFO configuration.

In the analogue three measurement setups were conducted for each hybrid type. These were developed for three types of CFO, to evaluate if the mirror signal from the mixing stage was properly filtered. These CFO frequencies were: 480 MHz, 600 MHz and 1020 MHz, with the VUBIQ frequency being adjusted for each case. These setups are displayed in the following figure.



(a) Type 1 with CFO of 480 MHz.

(b) Type 1 with CFO of 600 MHz.

(c) Type 1 with CFO of 1020 MHz.

(d) Type 2 with CFO of 480 MHz.

(e) Type 2 with CFO of 600 MHz.

(f) Type 2 with CFO of 1020 MHz.

Figure 4.40: Analogue hybrid measurements.

The performance characterisation for these measurements followed suit the method employed for the individual technologies, with IF and input power switched for the best case scenario and EVM measurements in both percentage and dB values conducted. A summary of these results is presented in table 4.14.

Table 4.14: Summary of results from analogue hybrid configurations.

Type	CFO	Intermediate Frequency	Input Power [dBm]	Analogue SNIR [dB]	$\overline{EVM}$ [%]	$\overline{EVM}$ [dB]
1	480	2	-11.72	12.78	97.48	0.14
		4	-13.51	7.88	36.35	-8.75
		6	-13.94	0.50	199.96	6.05
	600	2	-11.72	NA	NA	NA
		4	-13.51	7.55	179.73	5.12
		6	-13.94	9.50	22.91	-12.75
	1020	2	-11.72	NA	NA	NA
		4	-13.51	NA	NA	NA
		6	-13.94	13.05	30.19	-9.89
2	480	2	-11.72	NA	NA	NA
		4	-13.51	NA	NA	NA
		6	-13.94	NA	NA	NA
	600	2	-11.72	5.78	105.65	1.57
		4	-13.51	5.00	82.22	-0.85
		6	-13.94	7.17	101.06	0.48
	1020	2	-11.72	NA	NA	NA
		4	-13.51	NA	NA	NA
		6	-13.94	NA	NA	NA

These results displayed that due to the existence of mirror signals from both signal CFO and the insertion of a mixing stage, the received signal can not be properly decoded and in some cases can not even be recognized by the baseband processing unit.

Digital Approach

To eliminate replicas due to the Mixer and reduce the CFO, a digital approach was devised. This solution employs the VUBIQ as TX and the IT as RX, with 60 MHz CFO (TX_{f_c} = 59.94 GHz and RX_{f_c} = 60 GHz). The transmitting baseband signal is shifted 60 MHz to compensate for the system CFO and evaluate if this will result in a

properly decoded signal. In figure 4.41, the setup for this approach is displayed.

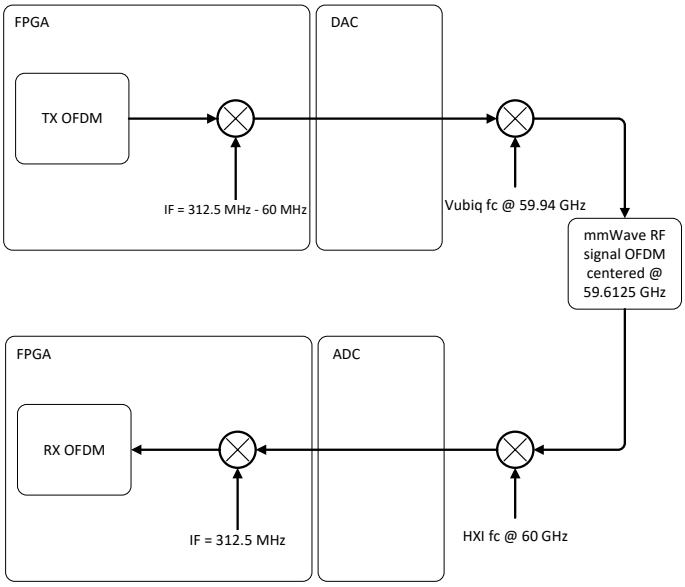


Figure 4.41: Setup for hybrid configuration with PEM009 TX and IT RX with 60 MHz CFO.

As with the VUBIQ and IT performance measurements, this method also evaluated its performance by measuring its SNIR and EVM values through varying its input power. A summary of these results are presented in the following table.

Table 4.15: Digital hybrid approach with PEM009 on TX and IT on RX with 60 MHz CFO.

Digital Gain	**Input Power [dBM]**	**Analogue SNIR [dB]**	$\overline{EVM}$ **[%]**	$\overline{EVM}$ **[dB]**
	-13.51	41.38	30.92	-10.06
7	-18.51	38.96	25.05	-11.86
	-23.51	37.03	**23.67**	**-12.40**

The received signal is shown in figure 4.42, where is seen that although the OFDM signal is present and distinguishable from the remaining spectra, a peak signal at 60 MHz is also present that interferes with the received signal quality. Furthermore, signal replicas and spurious signals are present around the OFDM signal null carriers which affect its performance.

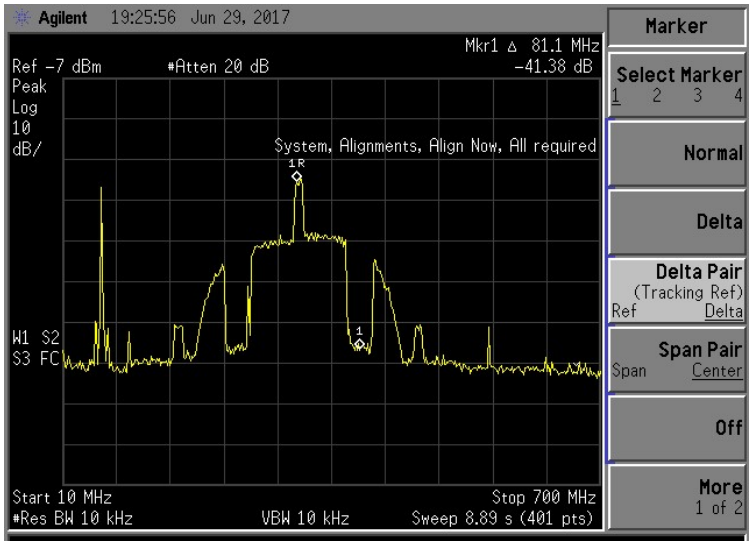


Figure 4.42: Received signal for digital hybrid configuration.

Chapter 5

A mmWave solution to provide AR in classrooms

In the scope of evaluating the system in a real-world user case, in the following section, the feasibility of this OFDM system in enabling an AR wireless transmission in a typical classroom environment, as seen in figure 5.1, is studied. This scenario intents to deliver multi-Gigabit/s of data transmission to multiple users (students) in LOS. As such, to guarantee the LOS between the transmitting antenna and the User Equipment (UE) and therefore mitigate the signal path loss associated with 60 GHz signals, a massive MIMO beamforming antenna array is employed. This array is connected to a server that is responsible for generating the virtual objects in the multiple OHMDs. In the receiver, an OHMD with a FPGA chip is responsible for the decoding, displaying and retransmission of inputs back to the server. FPGA chips are capable of providing the data processing requirements in an AR setting, while consuming up to 7x less power than modern Graphics Processing Units (GPUs) [2, 60]

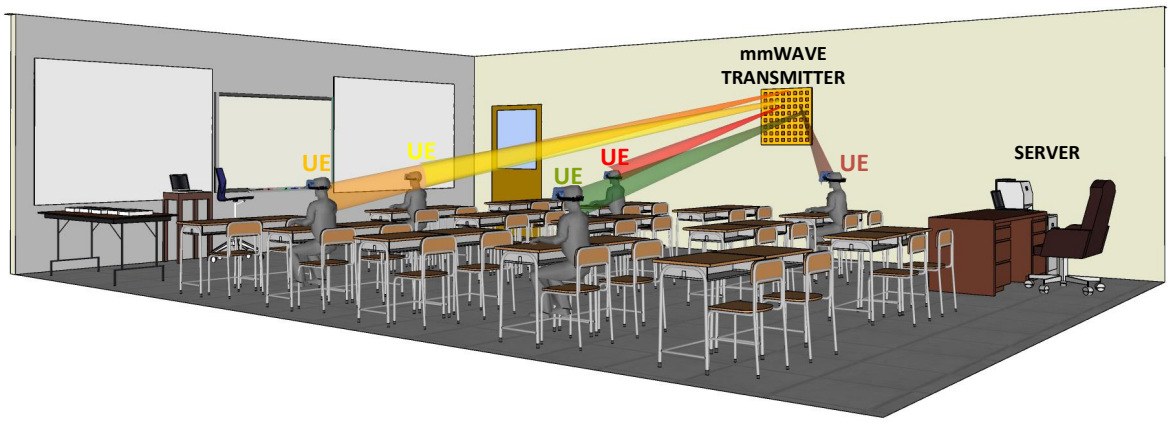


Figure 5.1: Proposed usage case scenario for AR applications in a classroom environment.

For this scenario, the VUBIQ PEM009 was used to evaluate the performance of the system in this scenario. While in the previous section it was established that the IT solution performed considerably better performance than the VUBIQ PEM009, this scenario is devised to be replicated in the future for a 2x2 MIMO solution. Therefore, the VUBIQ was chosen due to the availability of a second branch of this system. Furthermore, two baseband systems were used to mimic both transmitting and receiving processing.

5.1 Link budget assessment

In order to determine the system range, a link budget assessment was conducted on an anechoic chamber to mitigate multipath signal replicas. This was characterised for four different link distances of 0.5, 1, 2 and 4m. To improve the DAC and ADC reference clock signal stability, the rubidium clock source is connected to the reference clock input (CI) of the ADC. The DAC output signal (P_{DAC}) is connected to an analogue variable attenuator so that the TX input baseband level $P_{TX_{BB}}$ can be varied, and therefore the TX signal power level at mmWave is changed. The baseband received signal $P_{RX_{BB}}$ is then split to the ADC and the Agilent N9344C SA for EVM and SNR metric calculations, respectively. This assessment was conducted for an EVM threshold of -15 dB at the received signal since this is the minimum value required for 16QAM decoding. The transmitted power level was calculated, for each link distance, following 5.1.

$$P_{TX_{BB}} = P_{RX_{BB}} - G_{VUBIQ_{TX}} - G_{Ant_{TX}} + L_{PathLoss} - G_{AntRX} - G_{VUBIQ_{RX}} + IL, \quad (5.1)$$

where $G_{VUBIQ_{TX}}$ and $G_{VUBIQ_{RX}}$ are the VUBIQ TX/RX RF Front-ends, respectively, amplification gain, with $G_{VUBIQ_{TX}} = 6$ dB and $G_{VUBIQ_{RX}} = 43$ dB, $G_{Ant_{TX}}$ and $G_{Ant_{RX}}$ are the antenna gains for both TX and RX, with 25 dBi for TX and 0 dBi for RX, $L_{PathLoss}$ is the Friis free space path loss for the given distance and $IL = 9$ dB is the implementation loss from cable loss and equipment noise figures.

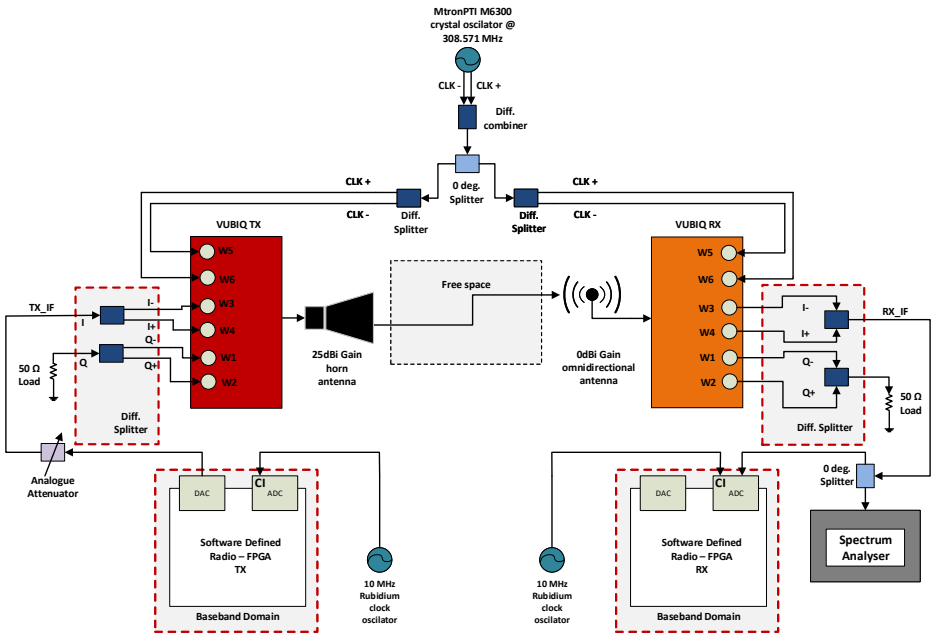
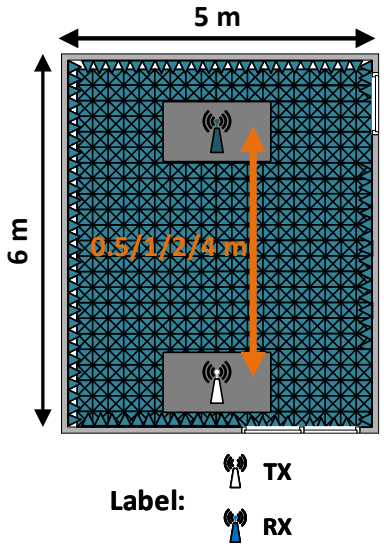
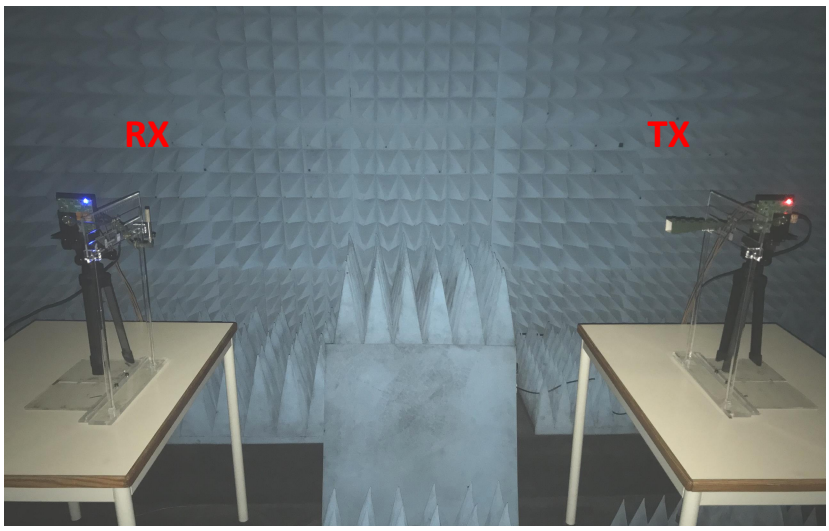


Figure 5.2: AR prototype system link budget assessment block diagram of the mmWave system setup.

The measurement setup was placed inside the anechoic chamber, as seen in figure 5.3, with the distance between antennas changed between the different scenario. Moreover, the system input power $P_{TX_{BB}}$ was altered according to the measured distance..



(a)



(b)

Figure 5.3: AR prototype system link budget assessment in anechoic: overall measurement setup (a) and picture (b).

For this measurement, a -15 dB EVM threshold was set as the threshold so that a higher modulation order, i.e. 16 QAM, can be used. The obtained results, for the different distances are shown in figure 5.4, where it is possible to determine that the current system is capable of being employed for the desired indoor setup (classroom). Furthermore, although the VUBIQ instability is present, the system provides enough operating range on each distance to compensate it.

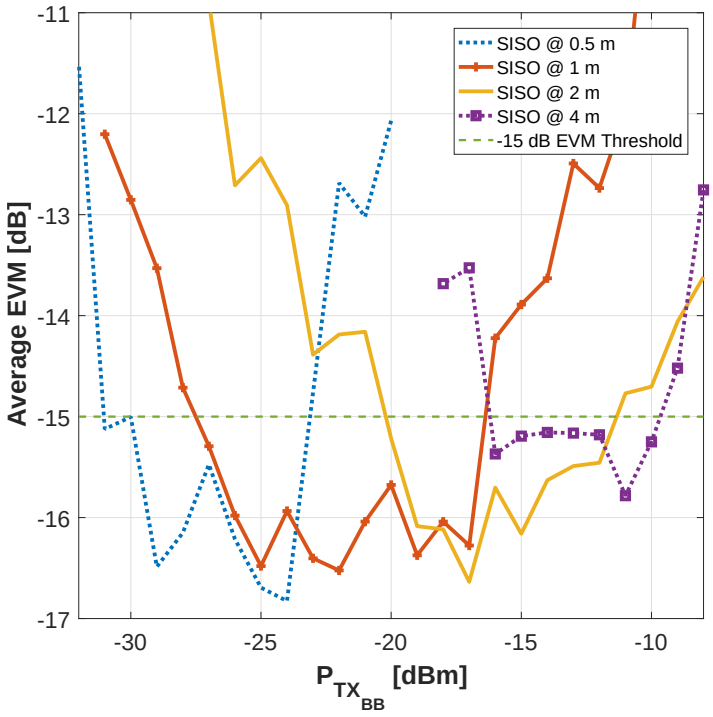
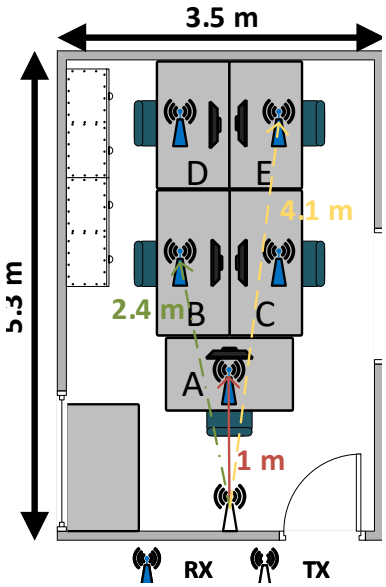


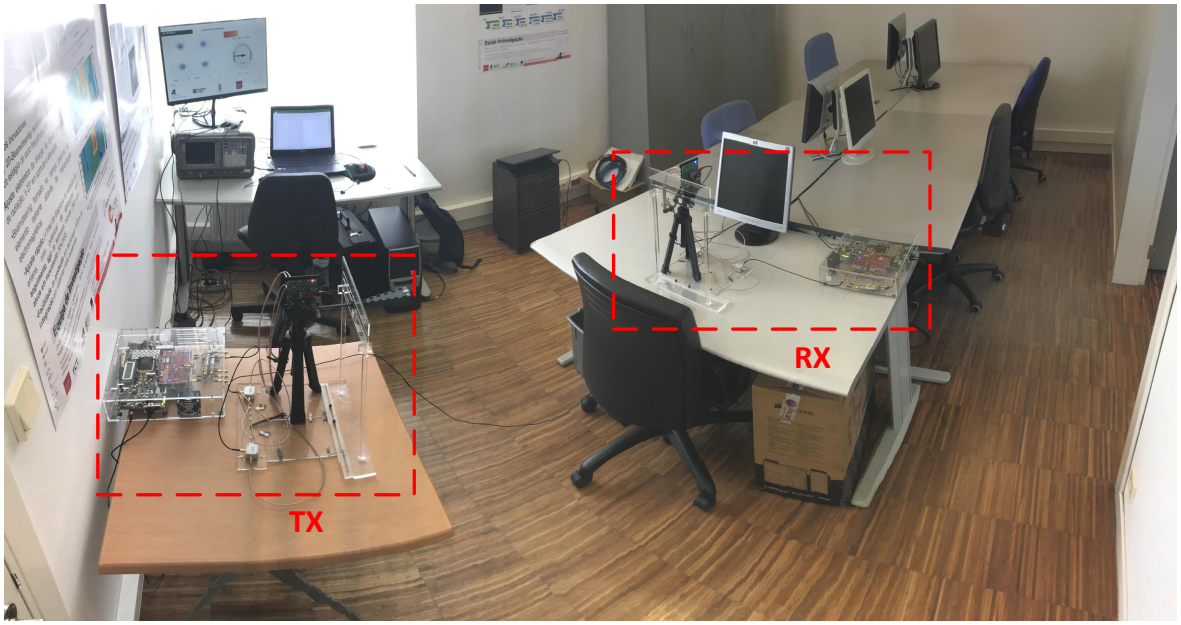
Figure 5.4: EVM versus $P_{TX_{BB}}$ for 0.5, 1, 2, and 4 m link distances.

5.2 Classroom assessment

For the real case scenario, a classroom, such as the one shown in figure 5.5a was used. This room has five tables that will be used to simulate five different UE's, labelled from A to E, for different TX-RX antennas and multipath scenarios. The real case setup is shown in figure 5.5b with the RX system placed on the A UE.



(a) Classroom measurement setup

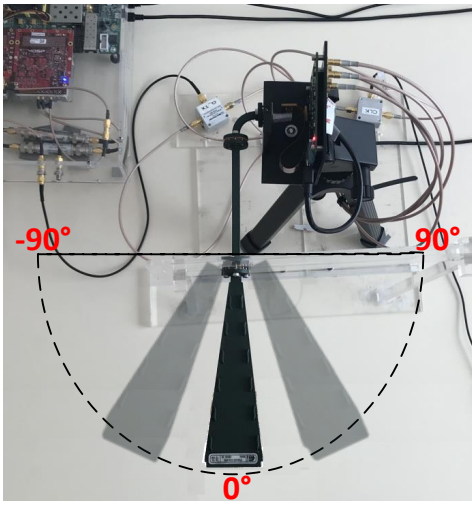


(b) Classroom measurement setup

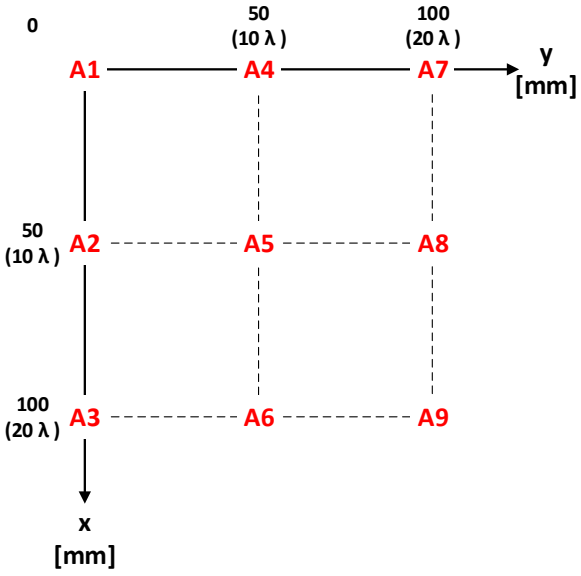
Figure 5.5: Classroom measurement setup

For the measurement of this setup, two FPGA's were used, one to act as the server and the other as the OHMD. Both TX and RX antennas were positioned at 1.1m from the floor, with UE antenna placed 40 cm high from the desk, to mimic the height of an OHMD device. From the previous link budget assessment, the equivalent isotropic radiated power (EIRP) was set to 9, 15 and 21 dBm for distances of 1, 2.4 and 4.1m, respectively. Additionally, since the development of the beamsteering multi-antenna structure is not within the confines of this work, the TX antenna was manually rotated to the LOS of each individual RX, as seen in figure 5.6a. The RX antenna was also

moved in each location following the matrix shown in figure5.6b. This matrix was set from the work developed in [61, 62] and it grants a measurement for the different multipath fading conditions due to the user's head movement.



(a)



(b)

Figure 5.6: Measurement setup in: (a) TX angular beam antenna coverage and (b) UE location matrix for A user.

Besides the different positions, a final test was conducted with a human sit between the TX and the UE to evaluate the interference caused by the presence of another user, as seen in figure 5.7. For this, the UE was placed on the E position with the human interferer on the C position. As with the previous cases, the TX antenna was rotated to the LOS of the UE, to lower possible multipath fading and interference from both the environment and the human user. In this setup, only 6 cases were considered, namely

the position E4 to E9.

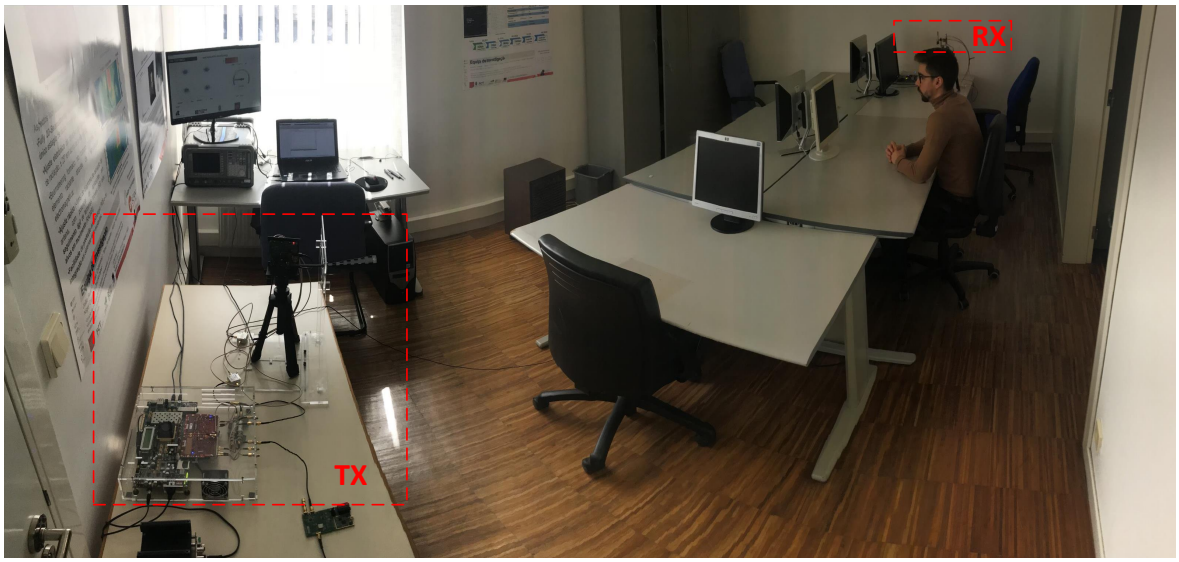


Figure 5.7: Measurement setup with human interferer.

For each position, 500 OFDM frames were measured to retrieve an average EVM value. Moreover, RX signal SNR and power were measured to evaluate the quality and path loss of the RX signal, respectively. From the final results, a cumulative distributive function (CDF) was computed from all the EVM results. The complete results figures can be seen on section E. From these, a compilation of these results were obtained for each UE.

Table 5.1: Field measurement results

User Equipment	**P_{TX} [dBm]**	$\overline{EVM}$ **[dB]**	$\overline{SNR}$ **[dB]**	**CDF of EVM at 50% [dB]**	**CDF of EVM at 90% [dB]**	$\overline{P_{ADC}}$ **[dBm]**	$\overline{PathLoss}$ **[dB]**
A	22	-16.15	28	-14.61	-8.8	-15.92	81
B	25	-14.08	28	-12.09	-9.3	-20.95	89
C	25	-14.57	30	-12.45	-8.4	-17.74	86
D	35	-13.83	29	-12.17	-8.5	-15.98	87
E	35	-14.76	30	-13.6	-10.4	-17.30	88
E + Human	35	-14.25	31	-13.36	-10.15	-18.01	89

In conclusion, this system was capable of providing the quality of service required to transmit at a data rate of 250 Mbps, which meets the expected data rates for a wireless AR system with the lower path loss case (User A) this was capable of reaching 500 Mbps. Furthermore, this was capable of providing coverage to all users, without

any interference resulting from the insertion of a human interferer for an edge case. As such, it can be concluded that this can be seen as a solution to current wireless systems limitations.

Chapter 6

Proposed MIMO block code

The proposed MIMO implementation was based on the transmitter diversity scheme introduced in [63]. Alamouti presents a solution for the transmission diversity in a 2x1 MISO system, while also showing how the decoding is conducted. Furthermore, a 2x2 decoding method is shown on this work. This implementation was conducted on a simulation level, more precisely on System Generator.

6.1 Proposed block diagram

The following work consists of a System Generator block code that will allow the current system to be scaled to a MIMO configuration, as shown in the following diagram.

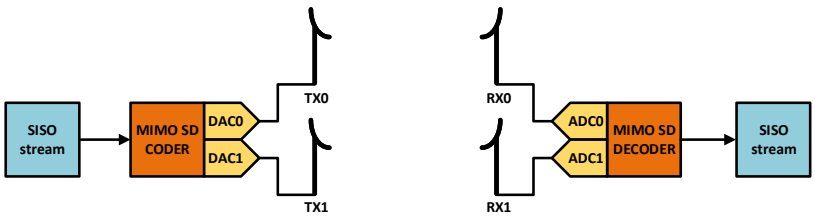


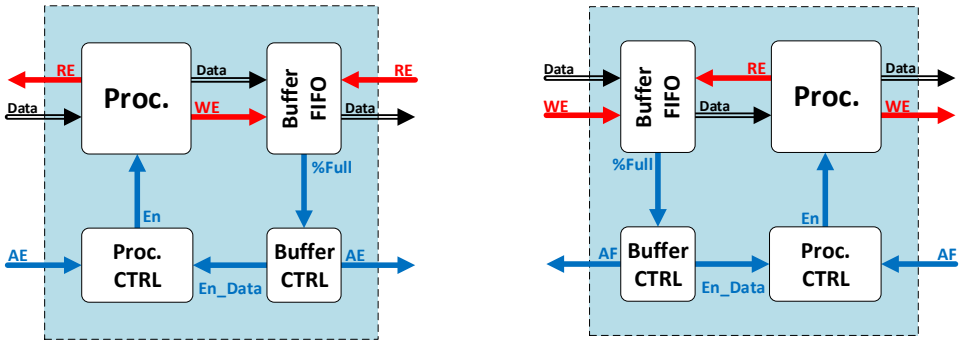
Figure 6.1: Block diagram of proposed MIMO block setup.

6.2 Baseband implementation at simulation level

The design architecture of this work is based on the work presented in [50]. This architecture is composed of different blocks that are asynchronous between each other through the use of First-In First-Out (FIFO) buffers that make the interface between

the different blocks. A block can be removed and inserted without disturbing the synchronism of the overall system, that is, this system can be described as modular solution. For the purpose of this work, a block code for both transmitter and receiver side were implemented to expand this SISO system to a MIMO solution.

Each block on the OFDM system is composed of the same four main components: processing unit, FIFO buffer and the controller units for both components. The processing unit is responsible for enabling the reading from the previous memory buffer through the Read Enable (RE) signal on the transmitter side and for the Write Enable of the data for the next block buffer FIFO on the receiver side. Furthermore, this block processes and writes or reads data from the block's buffer, whether it is a block on the transmitter or receiver, respectively. This processing is controlled by the processing controller which enables this block. The processing unit receives the control signal from the previous/next buffer controller that informs this block of the availability of data on the assigned FIFO, through the control signals Almost Empty (AE) or Almost Full (AF). If these signals are enabled, the Enable (En) signal to the processing unit is disabled and the processing is terminated until the next En signal appears. Furthermore, the processing unit controller receives an Enable Data (En_Data) signal from the buffer controller that is enabled when the FIFO occupancy level (%Full) does not exceed the 87.5% threshold on the transmitter and is not lower than the 50% threshold on the receiver. A template for both transmitter and receiver blocks is shown in the following figure.



(a) (b)

Figure 6.2: Block template for: (a) TX and (b) RX.

6.2.1 Alamouti 2x1

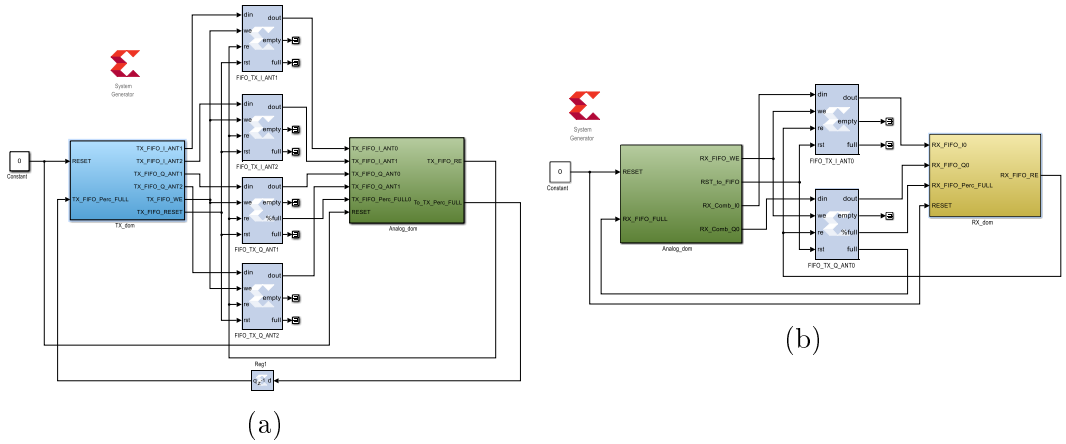
In this work, it was chosen to implement a MIMO diversity scheme based on the work presented in [63]. This diversity scheme is commonly known as Alamouti diversity

scheme, from its authors last name. This scheme presents a solution for transmission diversity in a MISO configuration. However, a 2x2 receiver scheme is also shown. This method is presented, collectively with the blocks implemented in System Generator. For the transmission scheme, the Alamouti code takes two adjacent symbols in time and encodes it for the two transmitting antennas. For example, the first two symbols of the data sequence (s_0 & s_1) are split to the two antennas on the same clock period. In the second clock period, the complex conjugate of these symbols are transmitted, with their assigned antenna inverted regarding the previous period. In the following table, a description of this scheme is presented.

Table 6.1: Encoding and transmission sequence for the two-branch Alamouti transmit diversity scheme.

Time \ **Space**	**Antenna 0**	**Antenna 1**
time t	s_0	s_1
time $t+T$	$-s_1^*$	s_0^*

This use of space (antennas) and time division for the transmission of data makes the Alamouti coding scheme a Space-Time Code Block (STBC). This can also be represented as a Space-Frequency Code Block (SFCB) by employing adjacent carriers instead of time adjacent symbols. The transmission scheme in Alamouti is invariable, whether a 2x1 or 2x2 configuration is employed. In figure 6.3, the 2x1 configuration on system generator is shown.

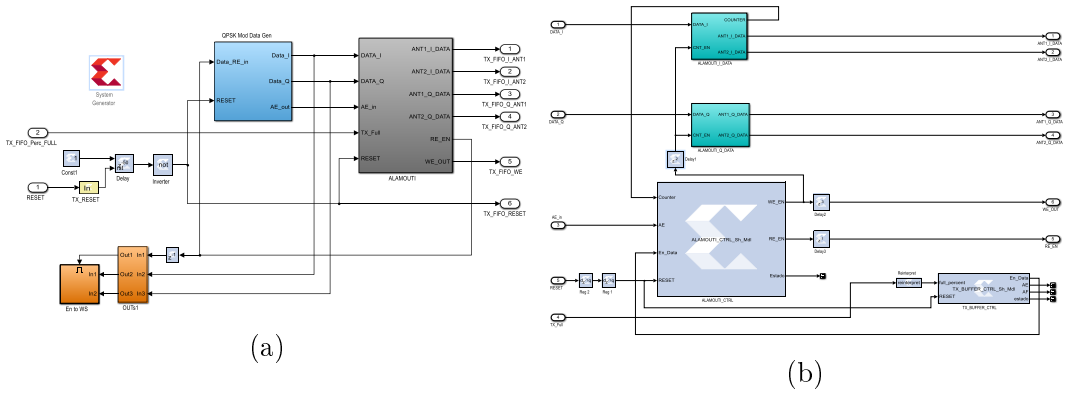


(a) (b)

Figure 6.3: Alamouti 2x1 transmitter diversity configuration on (a) TX side and (b) RX side.

To first perform measurements on the System Generator code, an initialization code sets the initial values for the different variables implemented, such as the clock domain

for both TX/RX and Analogue (channel) subsystems. for example, the clock domain on the Analogue subsystem is, by default, twice as slow as the one in the TX/RX cases. This system also splits the IQ signals in two separate $1+0i$ signals. As such, the deployment of the Alamouti transmitter must accommodate this feature and perform these actions separately. For the following figure, the overall and Alamouti encoder blocks are presented.:



(a) (b)

Figure 6.4: Alamouti TX block: (a) overall and (b) Alamouti coder.

The previous data generator block uses a read-only memory (ROM) whose data sequence is provided by the initialization code. This data is then passed through the Alamouti coder where it is generated the I/Q signals for the two antenna branches. In figure 6.5a, the coding for the I signals is shown. As seen in table 6.1, the output signal for the real part in the first clock period is $[s_0, s_1]$, for antenna 0 and antenna 1, respectively. For the second clock period, this is $[-s_1, s_0]$. As such, the input data stream is separated in two branches, for each transmitting antenna. To select the output bits, a counter block is employed. This block counts from 0 to 1 and is responsible for the selection of the multiplexer input. In the antenna 0, the first bit in the data stream (s_0) is passed through directly to the output and is then delayed for one clock period while it waits for the first bit in the antenna 1. In the second clock period, the inverted second bit ($-s_1$) is outputted to antenna 0. For the antenna 1, the first bit corresponds to the second bit in the data stream. To achieve this, the data on the first multiplexer input is delayed for two clock periods and therefore, the first data at the second multiplexer output is the second bit of data (s_1). Since the data on the antenna 0 is delayed for one clock period, both data streams ar now synchronised. In the third clock period, the second bit signal (s_0) is outputted and concatenated to the previous bit. This operation occurs for each two bit sets in the data stream for its entire duration.

In regards to the complex data stream (Q), the output bits for the first two bits

of data are $[s_0, s_1]$ for the antenna 0 and $[s_1, -s_0]$ for the antenna 1. As such, to perform this bit allocation, in antenna 0, the signals are transmitted directly, since no data computation is required, with only a delay inserted to guarantee the data synchronisation with antenna 1. As for the antenna 1, this is not the case, with the same method employed in the I data for antenna 1 used for this as well. However, the second output bit $(-s_0)$, besides being delayed for two clock periods is also inverted. This method is shown in figure 6.5b.

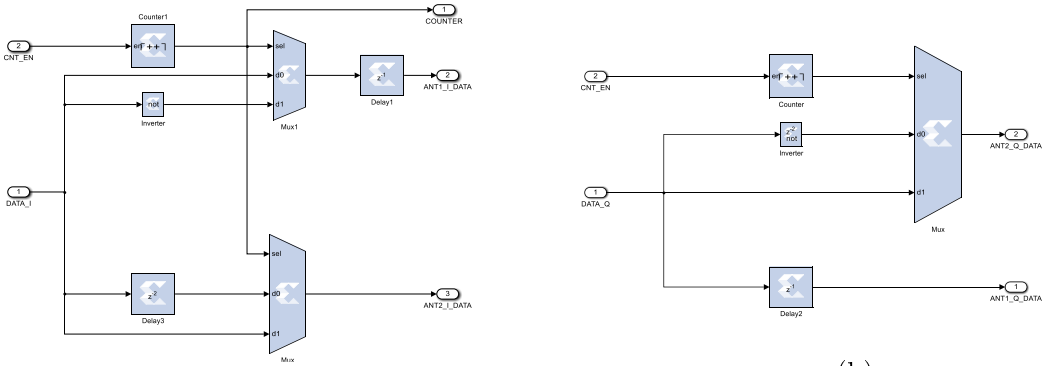


Figure 6.5: Alamouti coder on: (a) I and (b) Q data.

For the received signal, the transmitted signal is modeled by complex multiplicative distortions from the channel effect, as shown in the following equation

$$\begin{aligned} r_0 &= h_0 s_0 + h_1 s_1 + n_0; \\ r_1 &= -h_0 s_1^* + h_1 s_0^* + n_1, \end{aligned} \tag{6.1}$$

where r_0 is the received signal for the first bit period, r_1 is the received signal in the second bit period, h_0 and n_0 are the complex multiplicative distortion and receiver noise and interference from the antenna 0 and h_1 and n_0 are the complex multiplicative distortion and receiver noise and interference from the antenna 1. As such, to emulate the channel distortion (h_0, h_1), two data ROMs were introduced on the Analogue subsystem and here multiplied to the transmitted signal, as shown in figure 6.6. The result of this multiplication was then exported to the MATLAB workspace as a variable that is read on a ROM at the Analogue subsystem of the RX system.

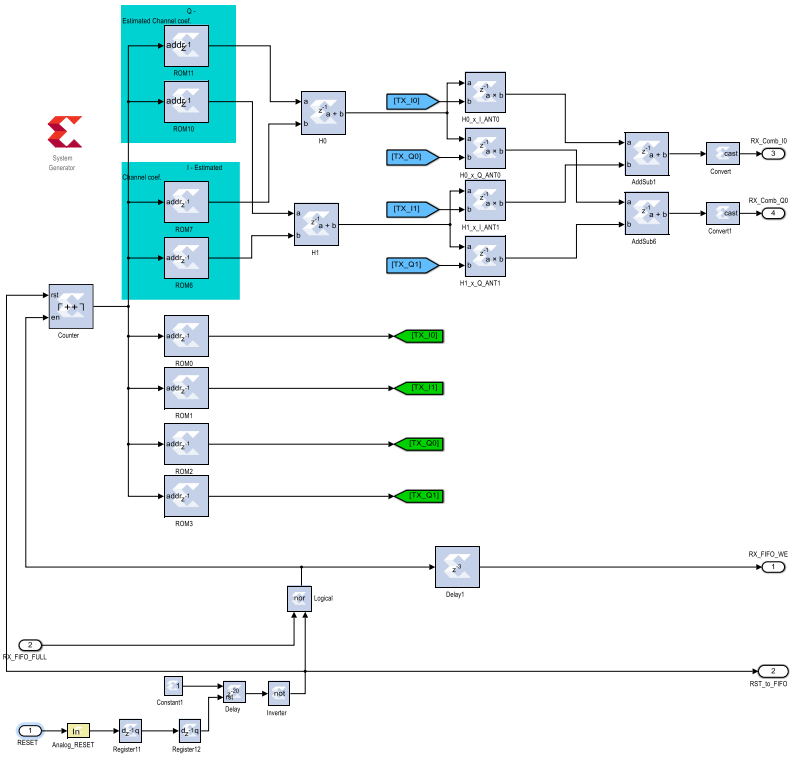


Figure 6.6: Analogue domain for Alamouti transmitter diversity scheme.

For the decoding of the data on the receiver, the decoded signals ($\tilde{s}_0, \tilde{s}_1, ..., \tilde{s}_N$, with N the data length-1) are given by the equations 6.2. Each decoded signal is composed of the combination of the both transmitted signals and the complex distortion associated. These are then passed through a decisor that will define what is the received signal. For a QPSK signal, the decisor defines if the received signal is higher or lower than 0 and establishes the correct amplitude to the signal.

$$\begin{aligned} \tilde{s}_0 &= h_0^* r_0 + h_1 r_1^*; \\ \tilde{s}_1 &= h_1^* r_0 - h_0 r_1^*. \end{aligned} \tag{6.2}$$

To perform the previous computation, the RX subsystem was parted in three sub-subsystems, as shown in figure 6.7. The first sub-subsystem (ALAMOUTI_DECODER_part1) is responsible for the multiplication of the complex channel coefficients in the received signal while the second (ALAMOUTI_DECODER_part2) is respomsible for the combining of the data streams form the previous block. As for the third block (Data_Decision_QPSK_only), this is responsible for the data decision for a QPSK signal.

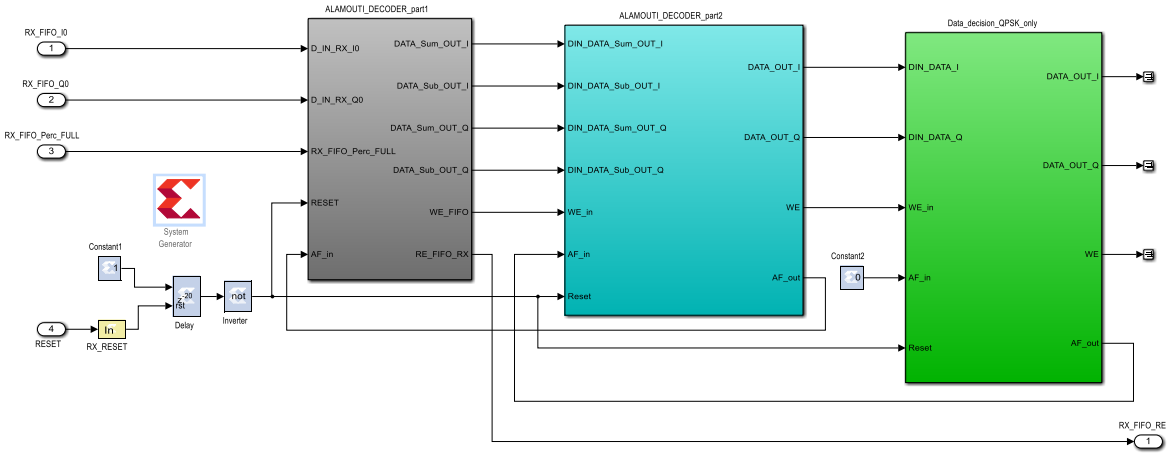


Figure 6.7: Alamouti RX sub-subsystems.

In the first block, channel coefficients are again multiplied to the received data, in both I and Q received signals. These generate two signals (Data_Sum) and (Data_Sub) that are combined on the next receiver block.

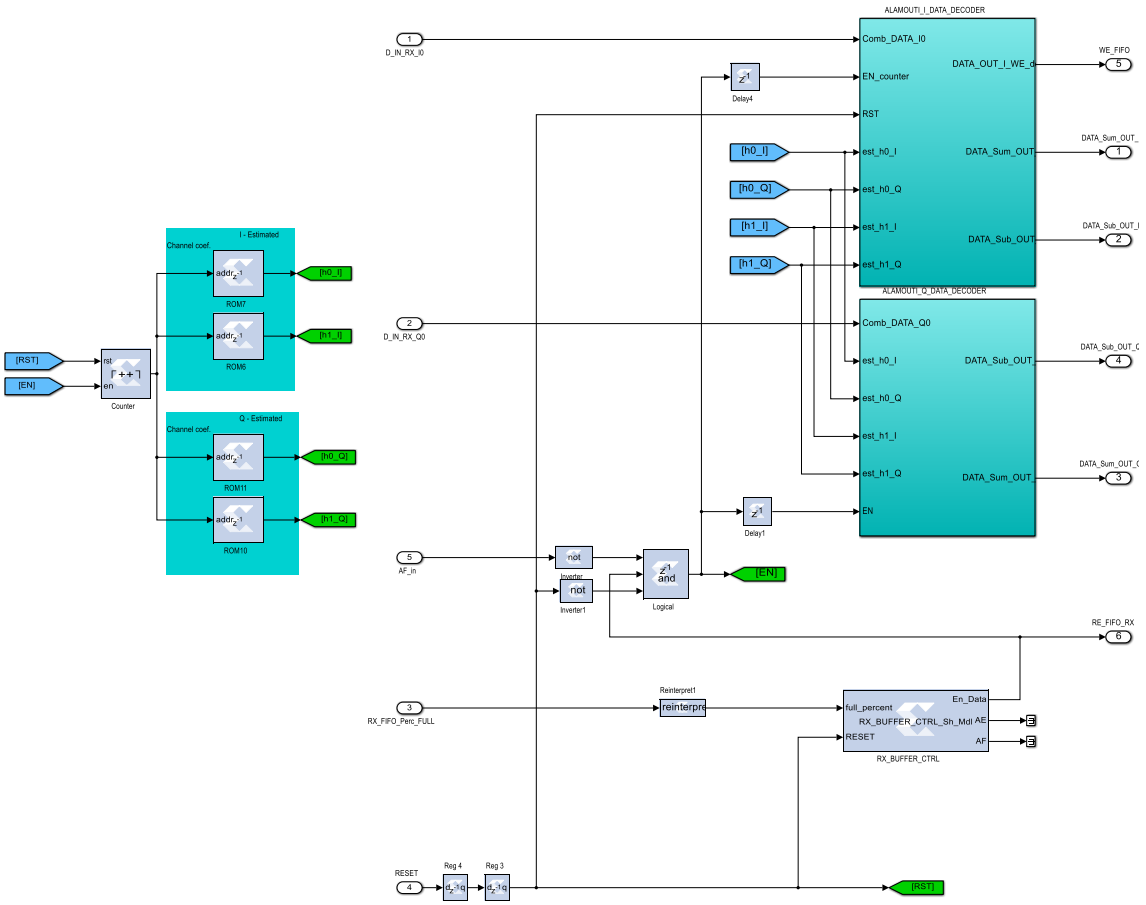
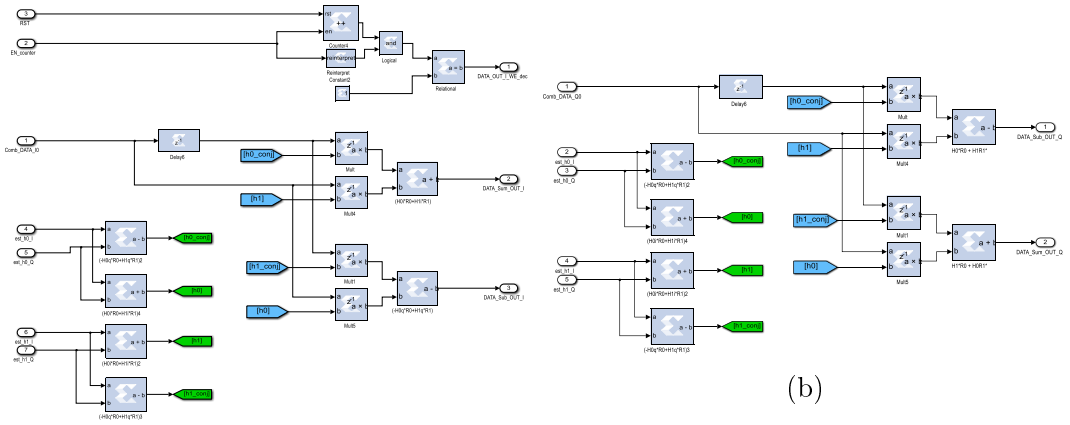


Figure 6.8: Alamouti RX ALAMOUTI_DECODER_part1 sub-subsystem.

For I signals, figure 6.9a, the received signal is split between four different channel coefficients, for the estimated and conjugated estimated complex distortions (h_0, h_1, $h_{0_{conj}}$, $h_{1_{conj}}$). To perform these computations, the signal is delayed for one bit period in the conjugated computations to guarantee the synchronisation with the estimated channel coefficients, which are computed with the second bit in the data stream (r_1). This decoding outputs two signals ($DATA\_Sum\_OUT_I, DATA\_Sub\_OUT_I$), which correspond to the first and second decoded bit for every two group of bits. As such, a selection between each output is requeired and performed on the following sub-subsystem.

For the Q signals, figure 6.9b, this computation is performed similarly to the I signals decoding. However the $DATA\_Sum\_OUT_Q$ is now generated by the computation of the estimated h_0 and conjugated $h_{1_{conj}}$, instead of the h_1 and $h_{0_{conj}}$ channel coefficients. Likewise, for the $DATA\_Sub\_OUT_Q$, the coefficients h_1 and $h_{0_{conj}}$ are now employed, due to the conjugated portion of the received signal.



(a) (b)

Figure 6.9: Alamouti decoder on transmitter diversity scheme on I data (a) and Q data (b).

The ALAMOUTI_DECODER_part2 sub-subsystem is responsible for the selection between the two input signals ($DATA\_Sum, DATA\_Sub$) in both I and Q signals. For this end, a controller was designed which is responsible for the FIFO RE signals, the enabling of the selecting multiplexers and the selection of the multiplexer input. This selection bit switches the multiplexer inputs every clock signal. For this, the RX_BUFFER_CNTRL_Sh_Mdl buffer controller reads the FIFO %Full signal and determines if this is between the established threshold, shown in 6.2. If this occurs, the En_Data is compared with the previous AF signal inversed, so that the data reading is enabled when both signals are 1.

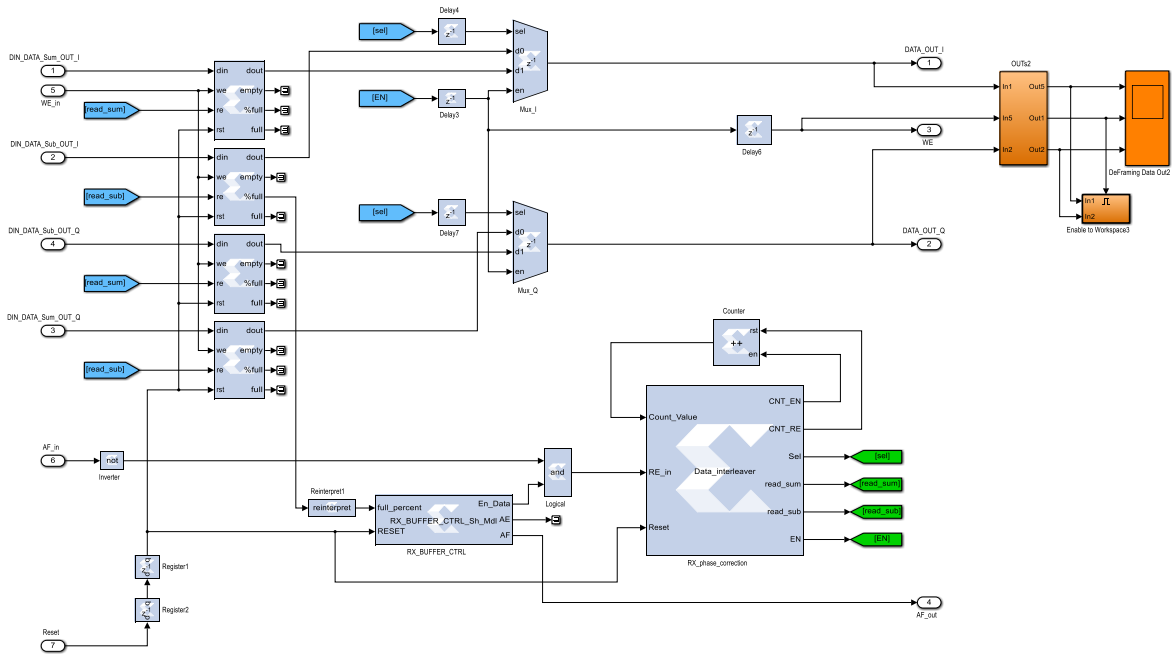


Figure 6.10: Alamouti RX ALAMOUTI_DECODER_part2 sub-subsystem.

For the final step, a data decision subsystem is employed that defines if the received signal is $+0.7071$ or -0.7071 for both I and Q signals, based on if their amplitude is positive or negative. The data decision block is currently only working with QPSK signals, however new decision blocks can be employed in future work for higher modulations.

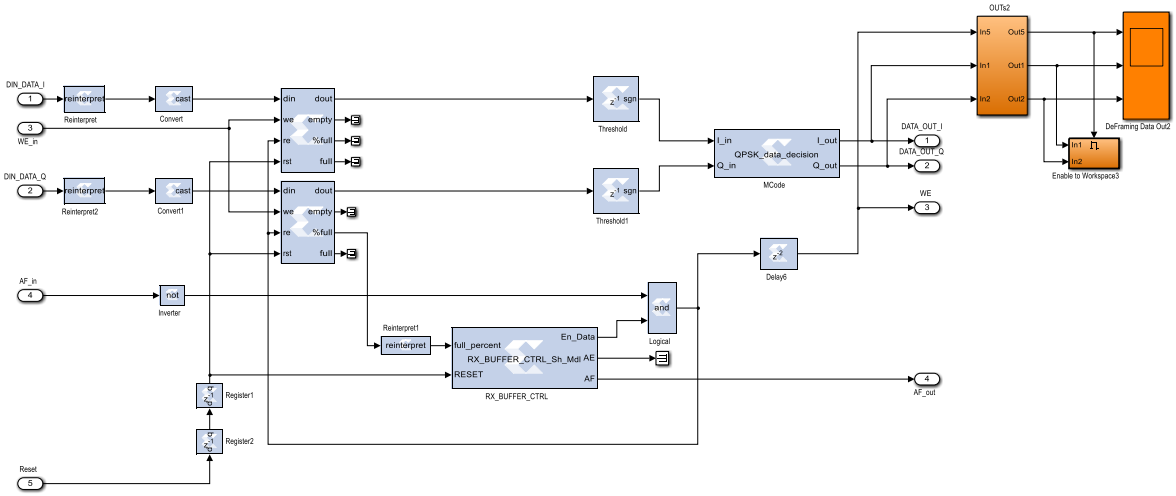
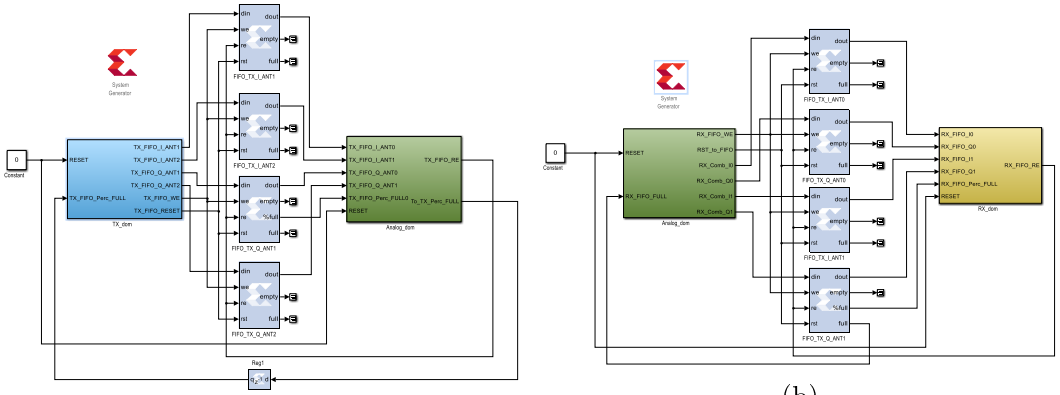


Figure 6.11: Alamouti RX Data_Decision_QPSK_only sub-subsystem.

6.2.2 Receiver diversity

The previous system employs the Alamouti transmission scheme shown in [63]. While this work aimed for a simple 2x1 transmission scheme, a receiver diversity decoding is also presented in this work. As such, this 2x2 scheme was also employed on System Generator blocks, as shown in the following figure.



(a) (b)

Figure 6.12: Transmitter side (a) and receiver side (b) on Alamouti transmitter and 2x2 receiver diversity configuration.

The transmitting scheme in this method remains the same as the one previously implemented, with only the receiver side altered. While in the previous scheme two channel coefficients were considered, in this new 2x2 system four channel coefficients are implemented, due to the effect on both transmitting antennas per each receiving antenna, as displayed in the following table.

Table 6.2: Channel coefficients allocation.

	RX antenna 0	**RX antenna 1**
TX antenna 0	h_0	h_2
TX antenna 1	h_1	h_3

Table 6.3 presents the received signals for both receiving antennas in the considered two clock periods. As seen, due to the increase in received signals, the complexity of the system as increased in comparison with the previous transmit diversity scheme.

Table 6.3: Received signals in space and time for receiver diversity scheme.

Time \ Space	RX antenna 0	RX antenna 1
time t	r_0	r_2
time $t+T$	r_1	r_3

where each received signal is determined as:

$$\begin{aligned} r_0 &= h_0 s_0 + h_1 s_1 + n_0 \\ r_1 &= -h_0 s_1^* + h_1 s_0^* + n_1 \\ r_2 &= h_2 s_0 + h_3 s_1 + n_2 \\ r_3 &= -h_2 s_1^* + h_3 s_0^* + n_3 \end{aligned} \tag{6.3}$$

In figure 6.13, the analogue receiver domain is displayed, with the different channel coefficients ROMs. These values, as with the transmitter diversity scheme, have been deployed through a workspace variable that generates random values.

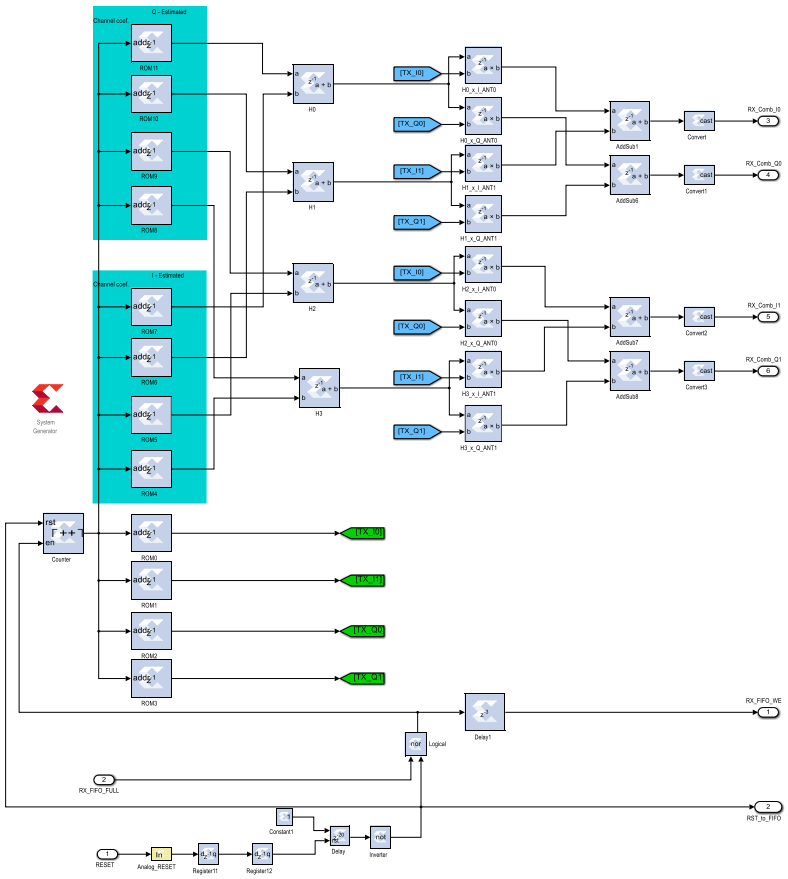


Figure 6.13: Analogue domain for Alamouti transmitter and receiver diversity scheme.

In order to properly decode the received messages, the following equation is employed:

$$\begin{aligned} \tilde{s}_0 &= h_0^* r_0 + h_1 r_1^* + h_2^* r_2 + h_3 r_3^* \\ \tilde{s}_1 &= h_1^* r_0 - h_0 r_1^* + h_3^* r_2 - h_2 r_3^* \end{aligned} \tag{6.4}$$

where, as with the 2x1 system, $\tilde{s}_0$ and $\tilde{s}_1$ represent the first and second received bits. Figure 6.14 shows the receiver ALAMOUTI_DECODER_part1 sub-subsystem. This system is responsible for properly decoding the received signal and employing the mathematical computation presented in equation 6.4. This outputs the sum and subtraction signals that are then assembled in the following subsystem.

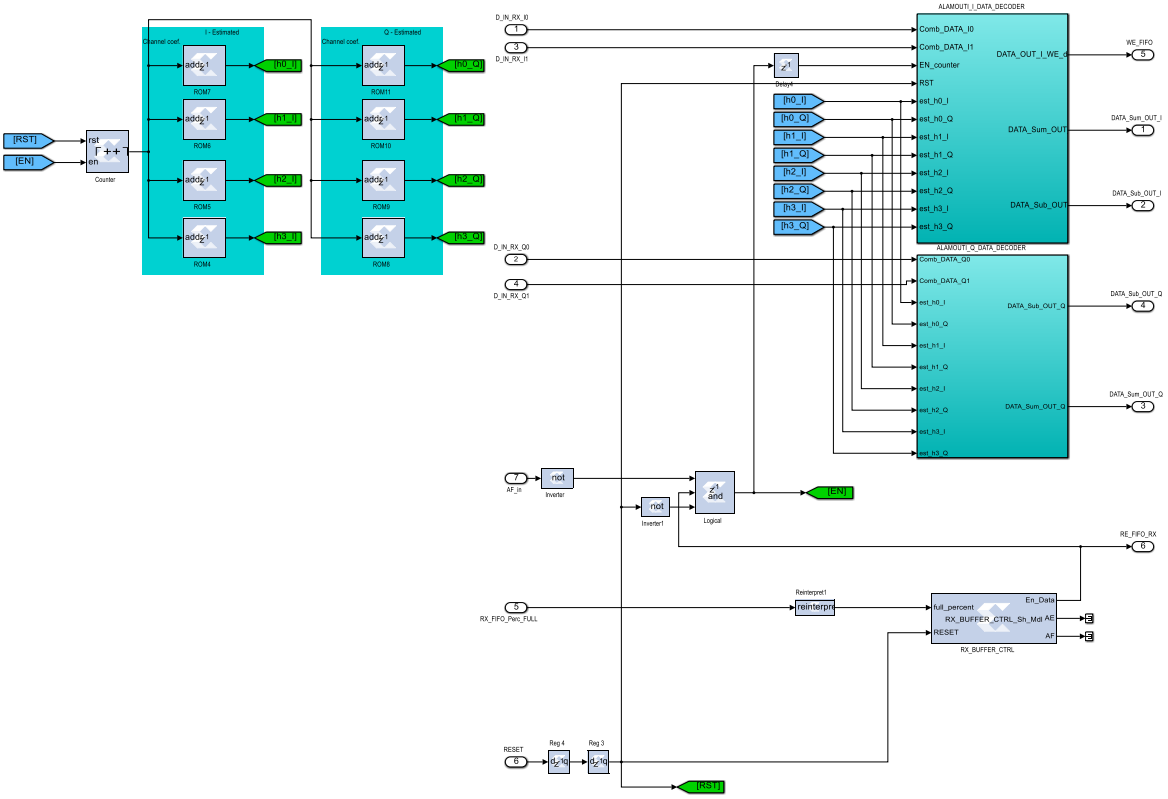
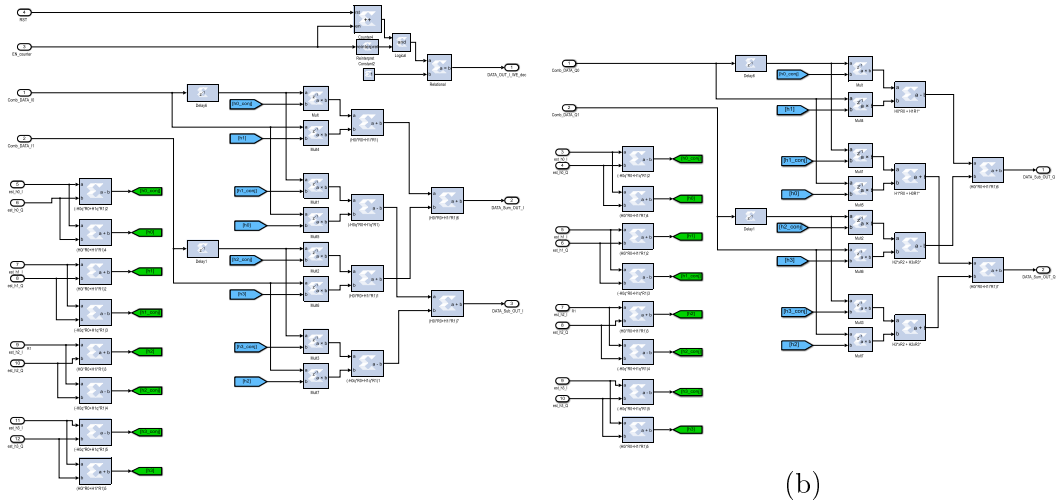


Figure 6.14: Alamouti RX ALAMOUTI_DECODER_part1 sub-subsystem.

The following figure displays the data decoding for both I and Q signals. This decoding stage functions in the same form as with the transmit diversity scheme, however the complexity of this subsystem has doubled from the previous one resulting form the insertion of another receiver branch.



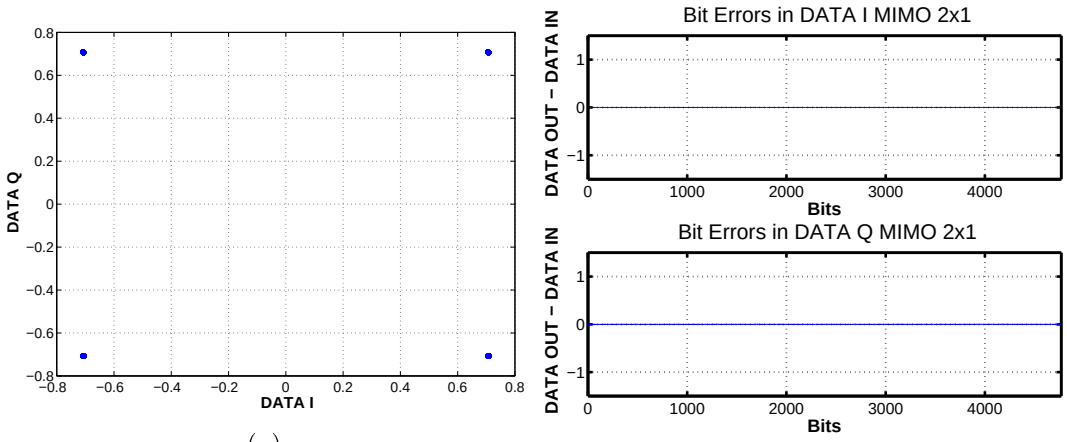
(a) (b)

Figure 6.15: Alamouti decoder on transmitter and receiver diversity scheme on I data (a) and Q data (b).

For this method, the subsequent block sub-subsystems (ALAMOUTI_DECODER_-part2, Data_Decision_QPSK_only) remain the same as the ones shown for the transmission diversity method. As such, between the two methods, only the first decoding part is changed, which allows for a simple switch between both types.

6.2.3 Results

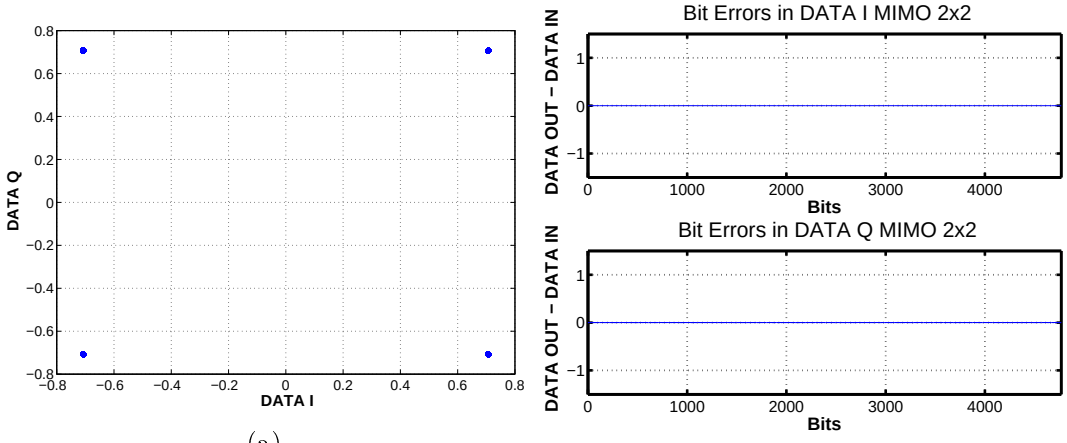
In the evaluation of the current system, only the random channel coefficients have been considered. To correctly perform a BER evaluation, a noise generator should be added at the end of the transmitter, which comes outside the scope of the current work. As such, to evaluate the system performance, a comparison between transmitted and received bitstream is performed. Furthermore, the received signal constellation was computed to verify the signal amplitude. In figure 6.16, the transmission diversity scheme is evaluated, while in figure 6.17, the receiver diversity results are shown.



(a) (b)

Figure 6.16: Received data results for 2x1 transmitter diversity scheme with: (a) received signal constellaion and (b) bit errors on received data.

From the previous figure is possible to conclude that the transmission diversity scheme does not show any bit error and as such was able to perfectly decode the transmitted bit stream, with the received signal constellation not presenting any signal distortion thanks to the QPSK decisor.



(a) (b)

Figure 6.17: Received data results for 2x2 receiver diversity scheme with: (a) received signal constellation and (b) bit errors on received data.

Figure 6.17 presents the receiver diversity results. These have performed as expected, with the received constellation not showing any bit deviation, which is confirmed by the null errors in the comparison between the transmitted and received signals.

While these systems have performed has expected in the simulation stage, the following step will be to migrate these to the current OFDM system and measure and

compare its performance with the previous SISO system. This, however, comes outside the scope of the current work and will be performed at a later stage. Furthermore, an evaluation of the current system BER performance will be also performed outside this work.

Chapter 7

Summary and conclusions

In this work, a full characterisation of a mmWave RF system was presented. This was based on measurements and performance evaluations at both baseband and RF front-end performed, which have showed that in the design of a wireless communication system, impairments on both stages can impact significantly the overall performance of the system. Furthermore, a comparison between COTS and a custom solution for RF Front-ends was performed. From this analysis, it was concluded that current COTS Front-ends are not capable of achieving the network data rate and stability demands for future wireless communication systems. Furthermore, a merge between both COTS and custom solutions is not feasible due to the CFO between both systems.

This system was also tested in a real-world scenario as a transmission method for a future wireless AR solution in a classroom. In this test, measurements of QoS metrics and performance evaluations were conducted in order to infer if this system was capable of providing enough data rate and quality of service for a real world multi-user AR solution. This was achieved, with the current system capable of providing adequate operating range to be used in a multi-user AR scenario with 250 Mbps/user with QPSK modulation. On the lower signal path scenario, higher modulation transmission schemes, such as 16 QAM, could be used to improve the overall data rate. Moreover, to improve the obtained results, a MIMO SD block code was developed in System Generator to be allocated to the current work and improve the system's signal resilience to path loss. This block code was designed for both transmission and receiver diversity, i.e. 2x1 and 2x2 schemes, respectively. The performance of these blocks was tested by implementing random generated values to the channel coefficients and it showed that no bit errors were obtained. In conclusion, the objectives of this work were achieved, with a thorough evaluation of the RF impairments of a 5G testbed performed and a real-world scenario benchmark performed. Furthermore, in the interest of improving and scaling the current work, a System Generator block code for an Alamouti diversity

scheme was developed and tested.

7.1 Future work

In this dissertation a full characterization of the impairments in a multi-gigabit solution were presented and its performance was assessed in a controlled and real-world environment. However, some future directions for this work were still left for future work.

- **Scaling the work to MIMO SD** - Although the MIMO block code has already been developed, its merge on the current system has no yet been completed;
- **MIMO performance measurement and comparison** - After the merge of the block code in the current system, a performance evaluation on both controlled and real-world scenarios is to be done, while having its results compared with the previous SISO solution;
- **Development of MIMO SM block codes and performance measurement** - To improve the system's overall data rate, the development of a MIMO SM block code will bring a solution for the doubling in data rate without increasing the modulation order. This should also be assessed and compared in the anechoic chamber and in a real use case scenario.

7.2 Contribution to Literature

The work presented in this dissertation has contributed to two submitted papers under review:

- R. Gomes, L. Sismeiro, C. Ribeiro, R. Caldeirinha, T. Fernandes, M. Sanchéz and A. Hammoudeh, Will COTS RF front-ends really cope with 5G requirements at mmWave?, *IEEE Access* [under second review];
- R. Gomes, L. Sismeiro, R. Caldeirinha, C. Ribeiro, M. Sanchéz and A. Hammoudeh, A mmWave solution to provide AR in classrooms, *15^{th} International Symposium on Wireless Communication Systems* [submitted].

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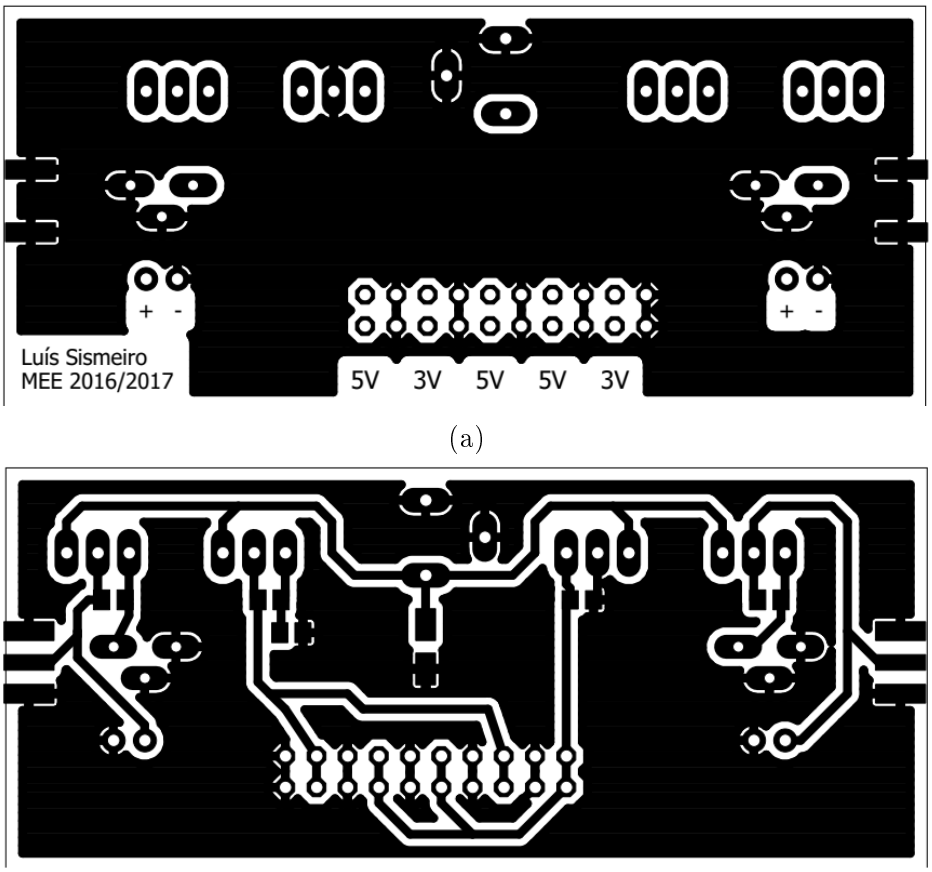
Appendix A

AGC

A.1 Power source PCB



(a)

(b)

Figure A.1: AGC power source PCB design layout: (a) top and (b) bottom.

A.2 AGC Case

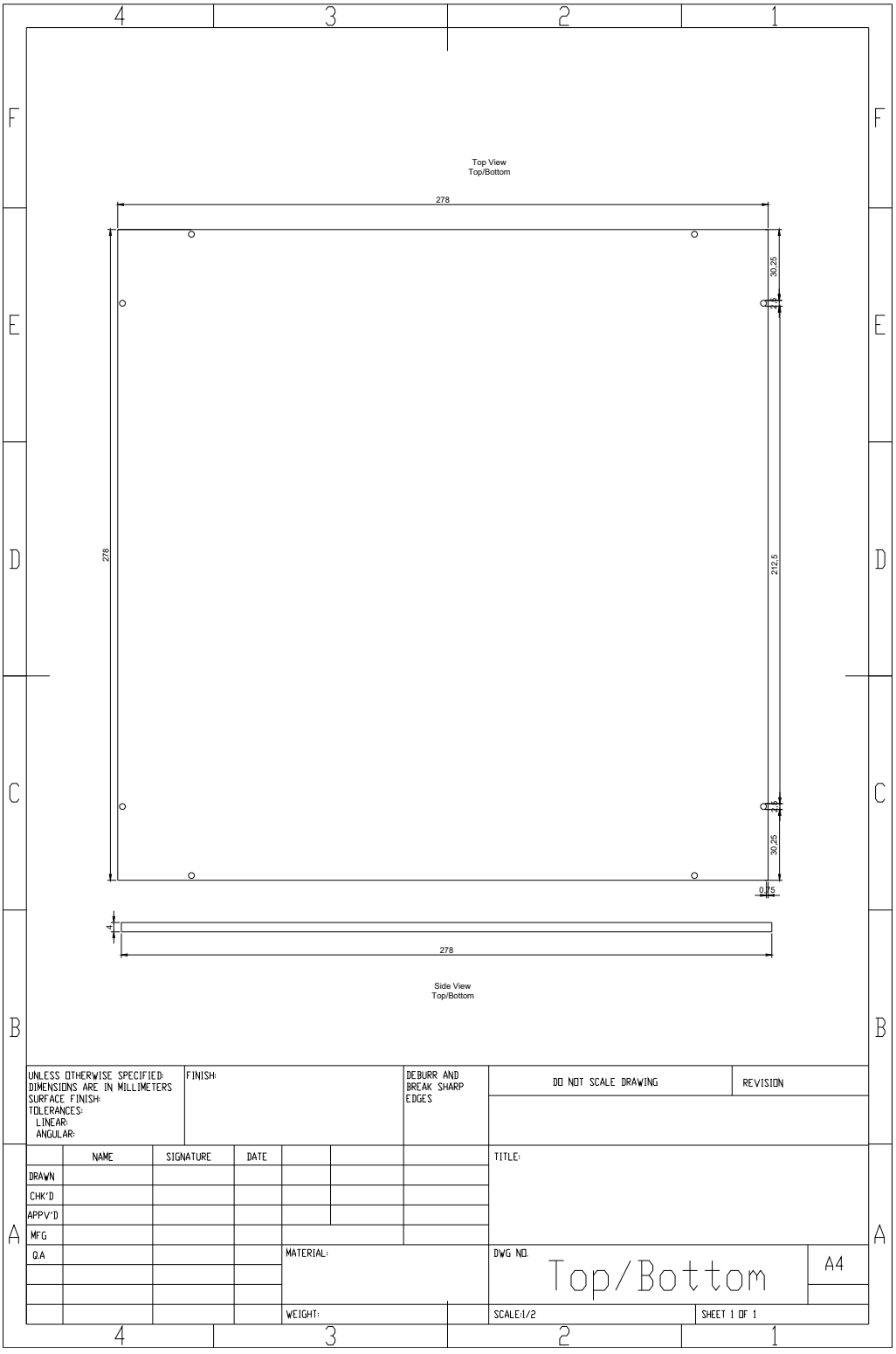


Figure A.2: Top and Bottom measurements for AGC acrylic box.

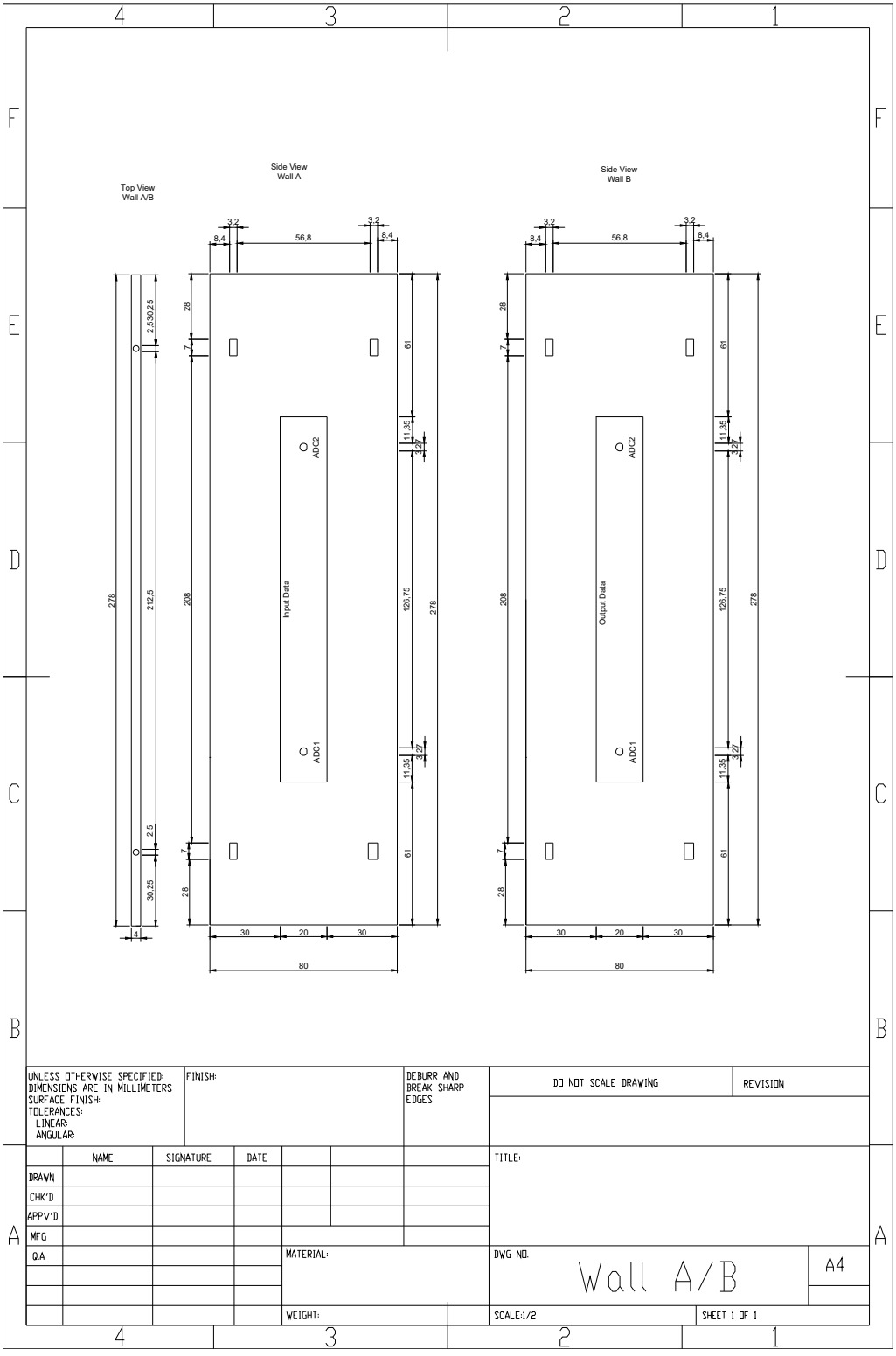


Figure A.3: Walls A and B measurements for AGC acrylic box.

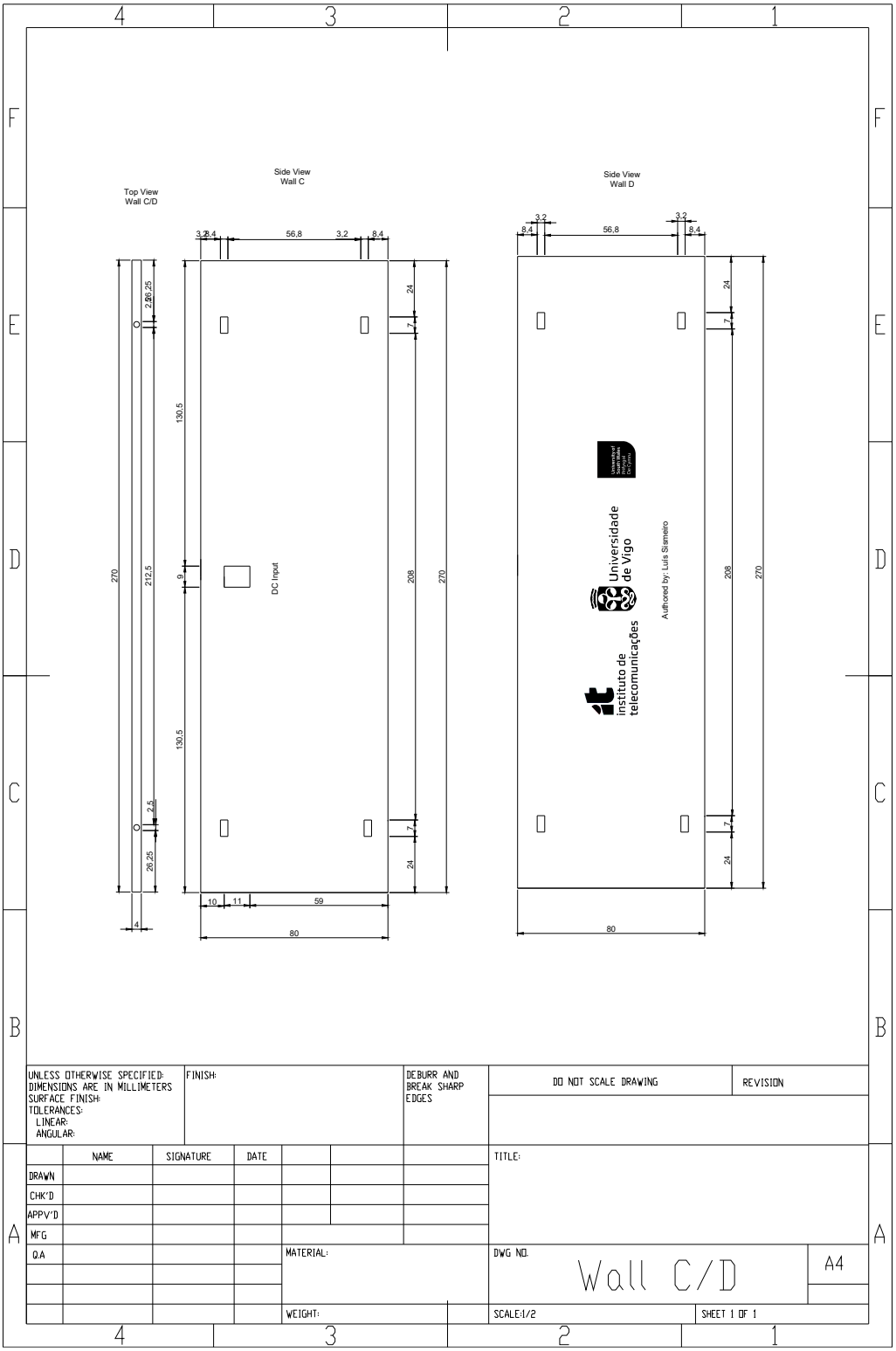


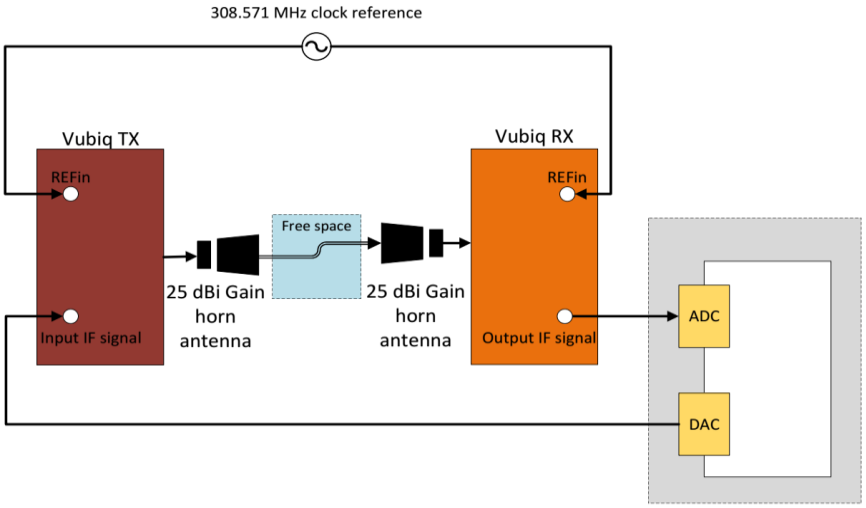
Figure A.4: Walls C and D measurements for AGC acrylic box.

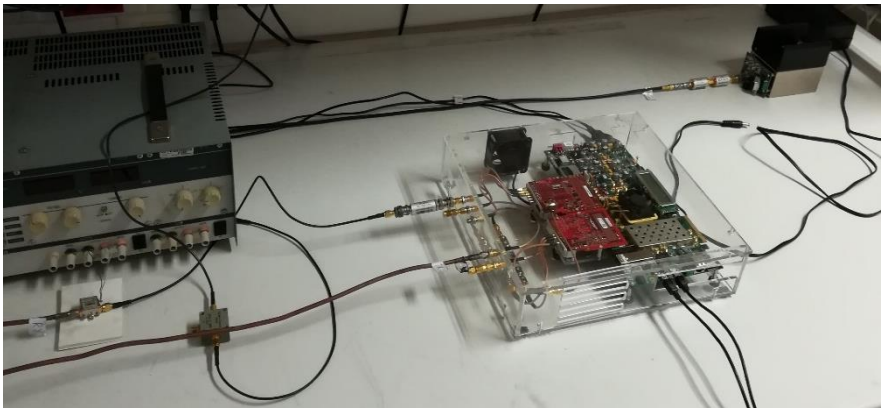
Appendix B

Manuals

In this section, the manuals for the measurement setup for both Vubiq and IT RF Front-Ends characterisation are shown, with the step-by step to perform and replicate the obtained results.

Vubiq-Vubiq Manual





Introduction

This document serves as the step-by-step guide for using the FPGA setup for transmit and receive signal while connecting its output and input to the Vubiq transmitter and receiver, respectively.

Step-by-step Guide

First Step - FPGA initialization

1) Connect the output DAC0 to the ADC0 of the input in order to test its back-to-back (B2B) configuration (always perform this step when initializing the FPGA);

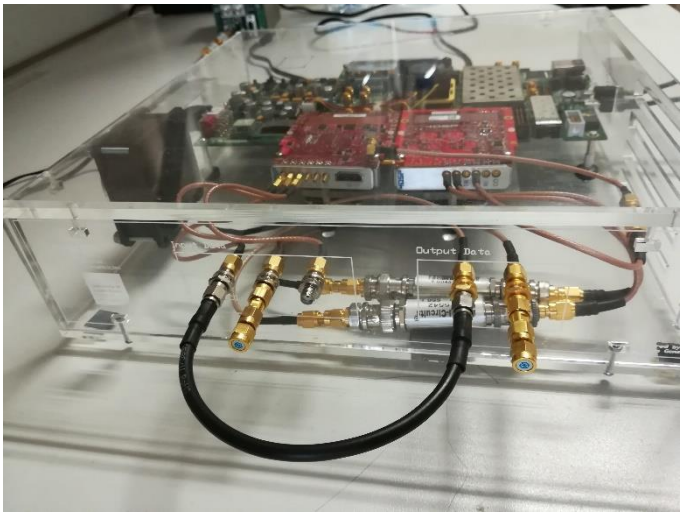


Figure 1 – Back-to-back configuration

2) Insert a 50 Ω termination on DAC1 and ADC1;

3) Open *Vivado 2015.2* and *Xilinx SDK 2015.2*;

4) On Vivado, select **Open Project** (Figure 1) and go to the designated folder (*OFDM_Vubiq_assessement\60GHz_OFDM_TRX\BB_OFDM_gain_project\BB_OFDM_gain*) and open the file *BB_OFDM_gain.xpr* (Figure 2);

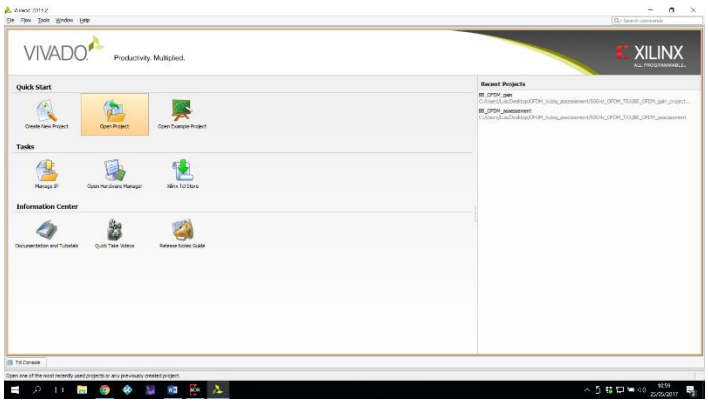


Figure 1 – Open Project on Vivado

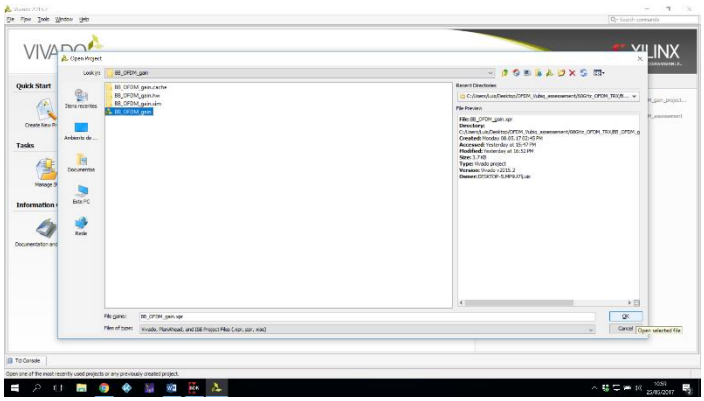


Figure 2 – Project Selection

5) Next, you will select **Open Hardware Manager** on the bottom left and select **Open Target → Auto-Connect**;

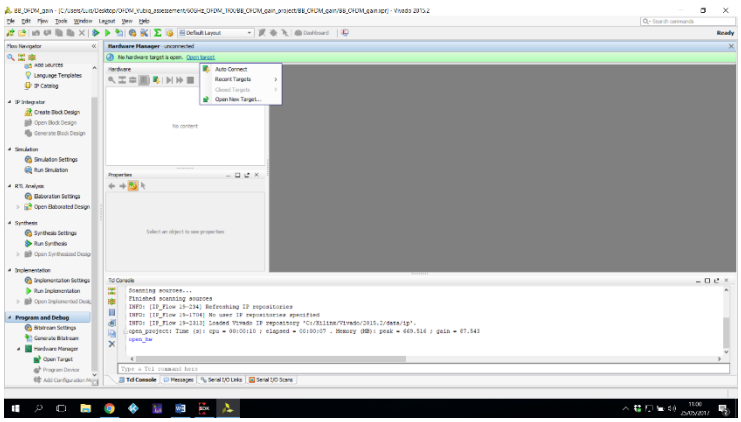


Figure 3 – Opening Target on Vivado

6) Then it will be required to program the FPGA, by choosing your bit and netlist files, found on *OFDM_Vubiq_assessement\60GHz_OFDM_TRX\Bit_stream_lower_sync_amp\60GHz_2_v2\Top_entity_wrapper.bit* and *OFDM_Vubiq_assessement\60GHz_OFDM_TRX\Bit_stream_lower_sync_amp\60GHz_2_v2\debug_nets*, respectively;

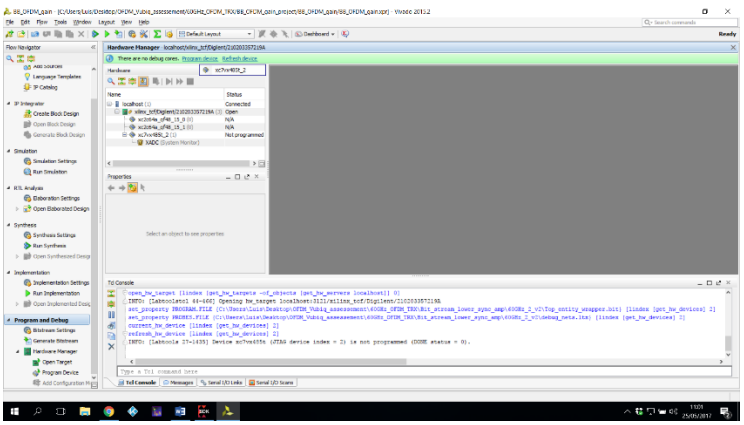


Figure 4 – Programming the device

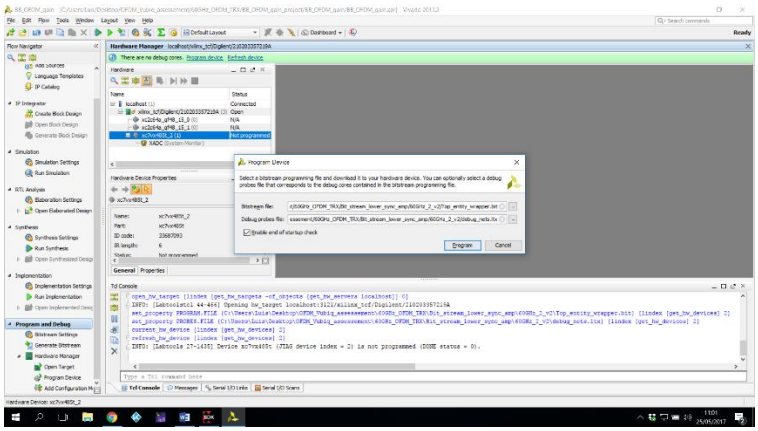


Figure 5 – File Selection for Programming the Device

7) Next, open SDK and select the following path: *OFDM_Vubiq_assessement\60GHz_OFDM_TRX\vc707_fmc126_vivado.sdk*;

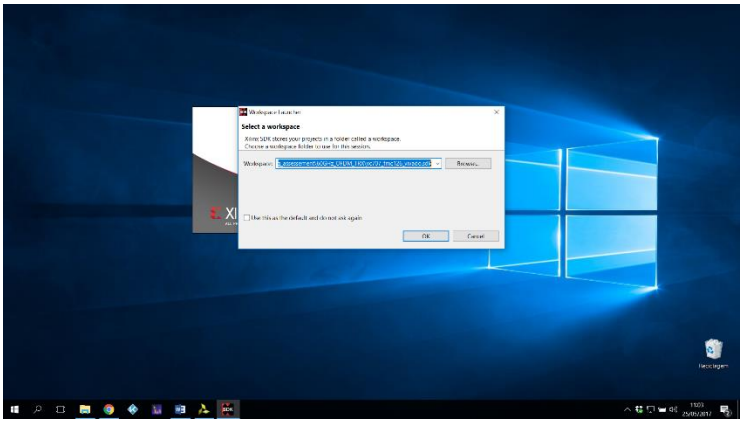


Figure 6 – SDK initialization

8) Then click on **Settings** on the terminal box and click **Run System Debugger** on the top to run the initialization of the setup. After this, program again your FPGA and see the results obtained;

9) Click on the button **SW4** on the FPGA in order to use the second configuration of IF available;

Figure 7 – Button Switches

10) Verify the results by clicking play on the Integrated Logic Analyzer (ILA) box. The ILAs are as follow:

- ILA 1 = Received Signal;
- ILA 2 = Channel Estimation and IF value;
- ILA 3 = Gain;
- ILA 4 = Transmitted Signal.

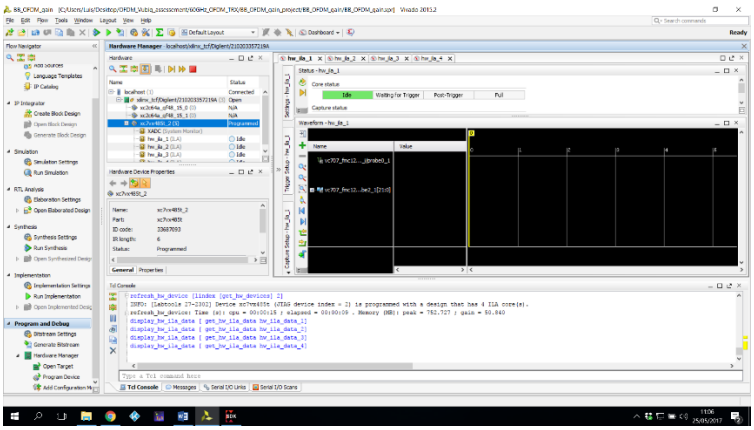


Figure 8 – ILAs at the Vivado workspace

11) After running each ILA, verify ILA1 and make sure that the synchronization signal is correct. If not, verify if the value on ILA 2 is 2.

12) If the system is not working, verify the connections and program the device again. Make sure IF is 2 when analysing ILA 1. Repeat this process until obtaining the expected results;

13) The click on **Tools → Run Tcl Script…** and select **medicoes.tcl** on the following path: *OFDM_Vubiq_assessement\3-EVM_BER*;

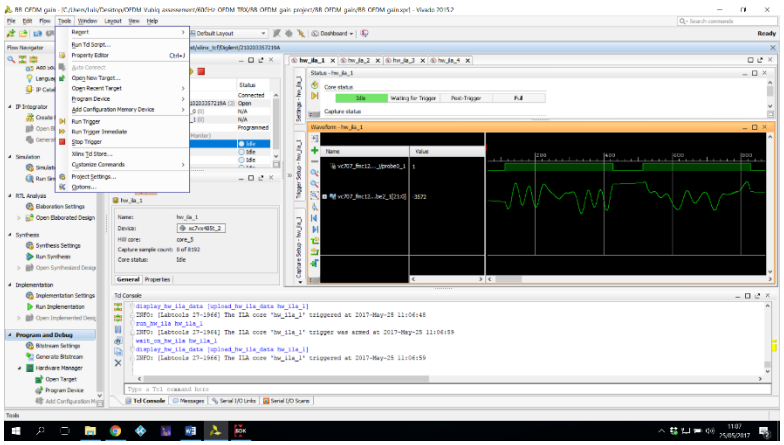


Figure 9 – Running Tcl files

14) Verify the results by running the Matlab script ***VIVADO_ILA_EVM_tester.m***, with the capture directory being *OFDM_Vubiq_assessement/3-EVM_BER/Measurements/VUBIQ_60GHz/*;

15) Repeat this test with different values of gain until its maximum value of 7, in order to achieve maximum value of Signal-to-Noise Ratio (SNR).

Second Step – Vubiq Integration

1) Make the following connections, presented in figure 10;

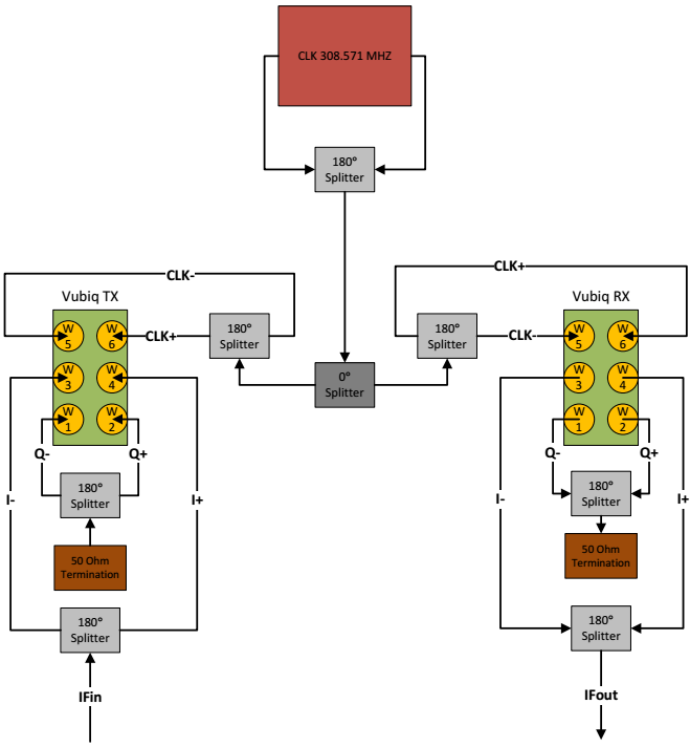


Figure 10 – Connections for the Setup

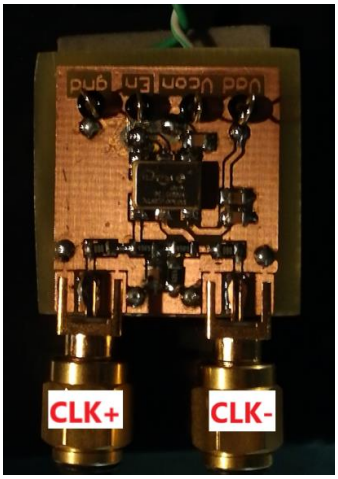


Figure 11 – Clock configuration

2) Connect the USB cable from the Tx and Rx Vubiq and run the RegisterGUI.exe on the Gui 1.95 folder. Make sure that both Attenuators are at 20 dB. Save and exit;

3) Connect the USB cables to the USB power sources;

4) Let the Vubiq stabilize for 15 minutes and make a capture;

5) Adjust the height and direction of one of the antennas, in order to maximize the SNR value;

6) Run the tcl script and test the results on Matlab.

IT-IT Manual

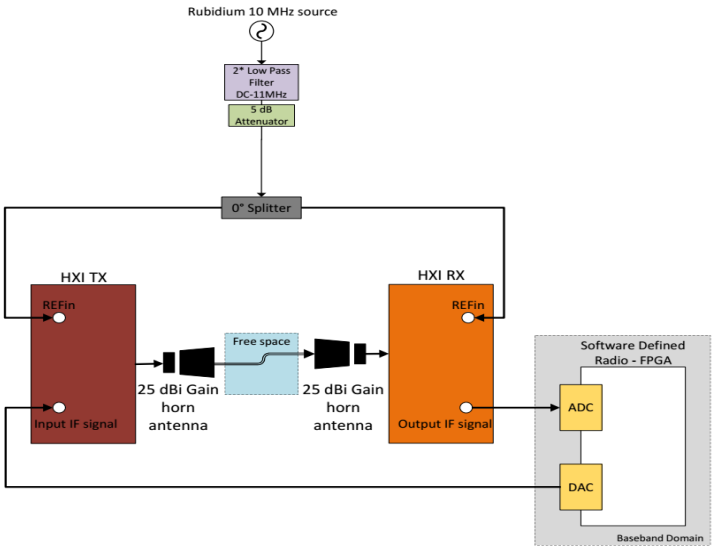


Figure 1 – System Overview

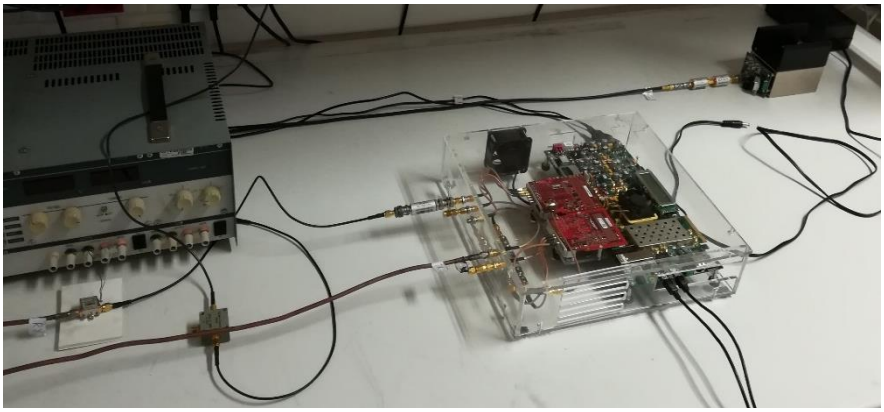


Figure 2 – Baseband Setup

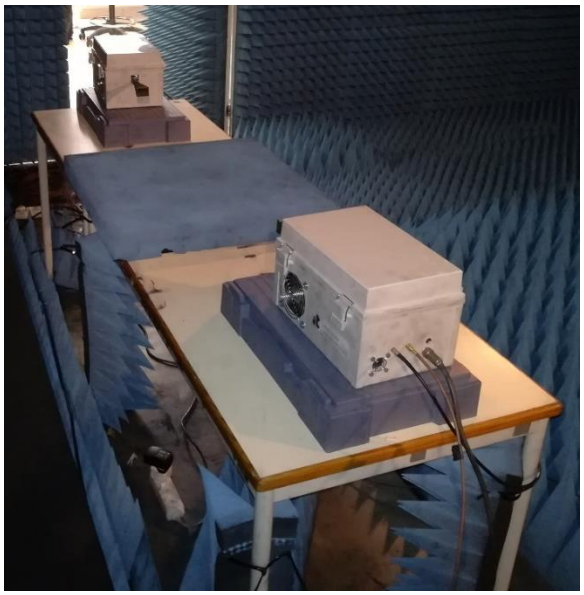


Figure 3 – IT Boxes Setup

Introduction

This document serves as the step by step guide for using the FPGA setup for transmit and receive signal while connecting its output and input to the HXI transmitter and receiver, respectively.

Step-by-step Guide

First Step - FPGA initialization

1) Connect the output DAC0 to the ADC0 of the input in order to test its back-to-back (B2B) configuration (always perform this step when initializing the FPGA);

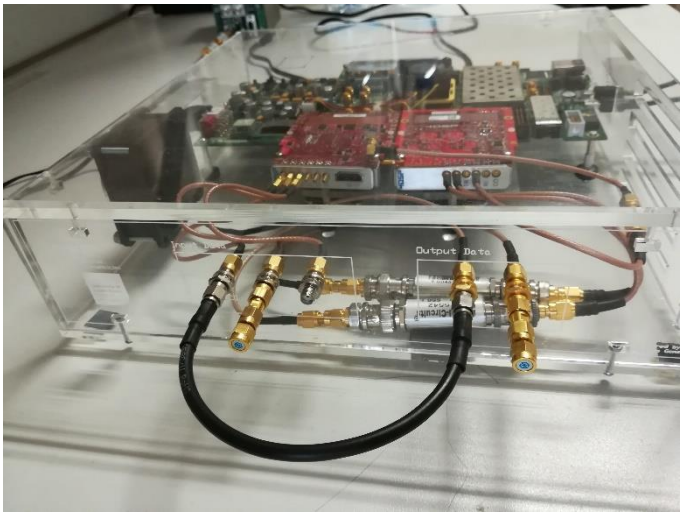


Figure 4 – Back-to-back configuration

2) Connect a 50 Ω termination on DAC0 and ADC0;

3) Open *Vivado 2015.2* and *Xilinx SDK 2015.2*;

4) On Vivado, select **Open Project** (Figure 1) and go to the designated folder (*OFDM_Vubiq_assessement\60GHz_OFDM_TRX\BB_OFDM_gain_project\BB_OFDM_gain*) and open the file *BB_OFDM_gain.xpr* (Figure 2);

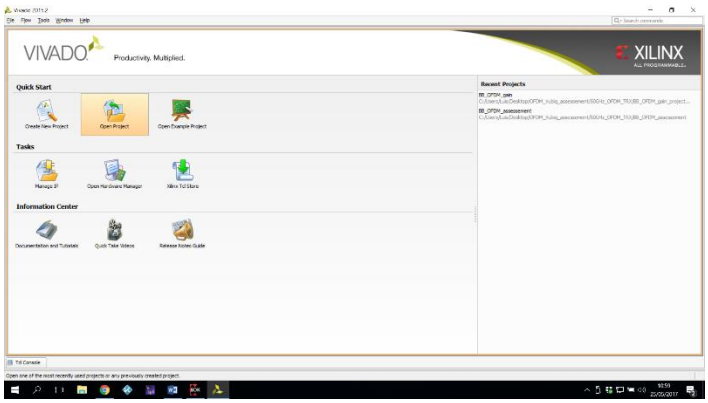


Figure 5 – Vivado Initial Workspace

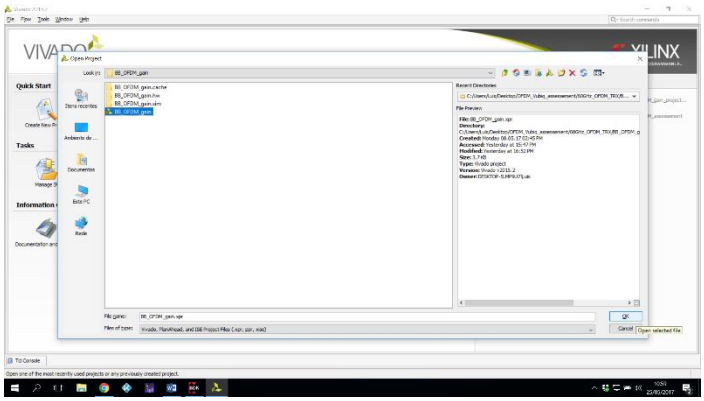


Figure 6 – Project Selection

5) Next, you will select **Open Hardware Manager** on the bottom left and select **Open Target → Auto-Connect**;

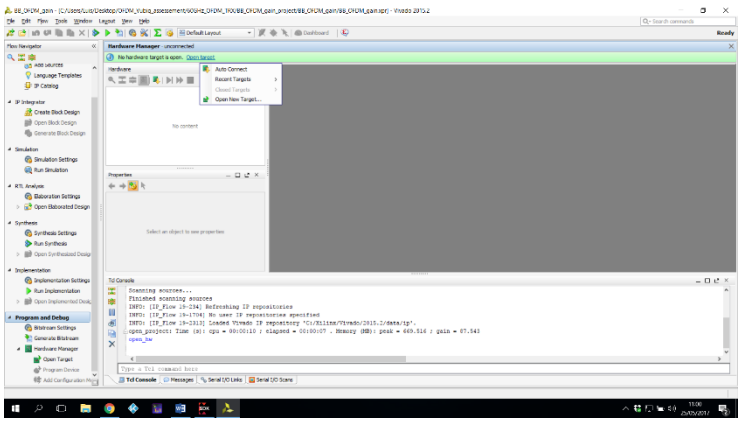


Figure 7 – Opening Target on Vivado

6) Then it will be required to program the FPGA, by choosing your bit and netlist files, found on *OFDM_Vubiq_assessement\60GHz_OFDM_TRX\Bit_stream_lower_sync_amp\60GHz_2_v2\Top_entity_wrapper.bit* and *OFDM_Vubiq_assessement\60GHz_OFDM_TRX\Bit_stream_lower_sync_amp\60GHz_2_v2\debug_nets*, respectively;

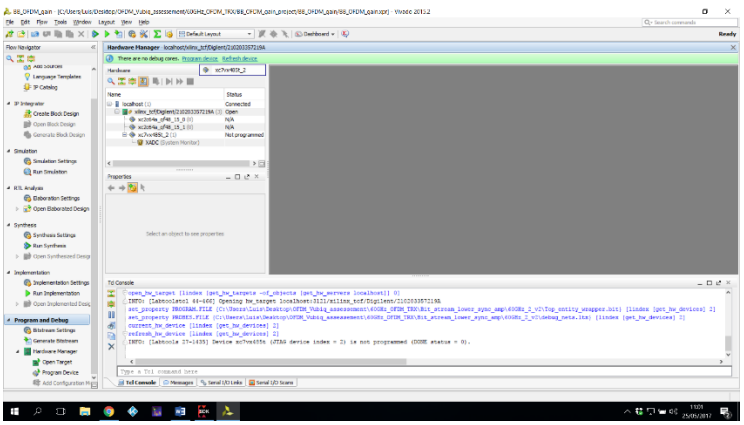


Figure 8 – Programming the device

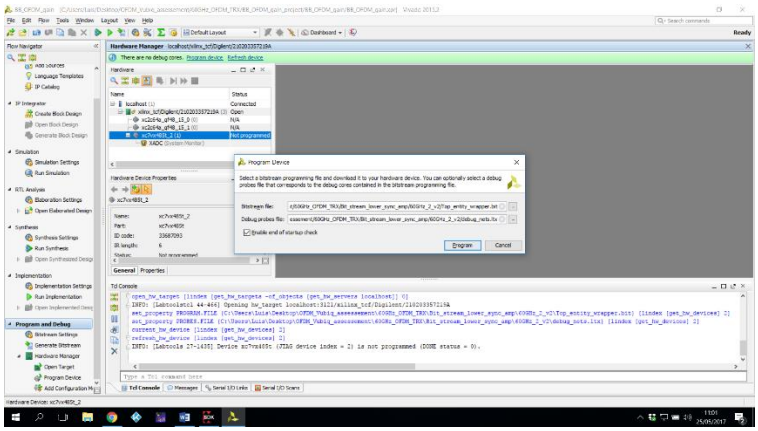


Figure 9 – File Selection for Programming the Device

7) Next, open SDK and select the following path: *OFDM_Vubiq_assessement\60GHz_OFDM_TRX\vc707_fmc126_vivado.sdk*;

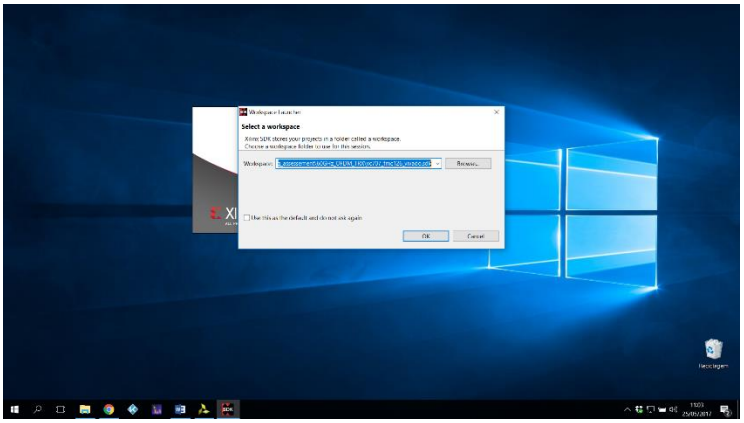


Figure 10 – SDK initialization

8) Then click on **Settings** on the terminal box and click **Run System Debugger** on the top to run the initialization of the setup. After this, program again your FPGA and see the results obtained;

9) Click on the button **SW4** on the FPGA in order to use the second configuration of IF available;

Figure 11 – Button Switch on the FPGA

10) Verify the results by clicking play on the Integrated Logic Analyzer (ILA) box. The ILAs are as follow:

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- ILA 3 = Gain;
- ILA 4 = Transmitted Signal.

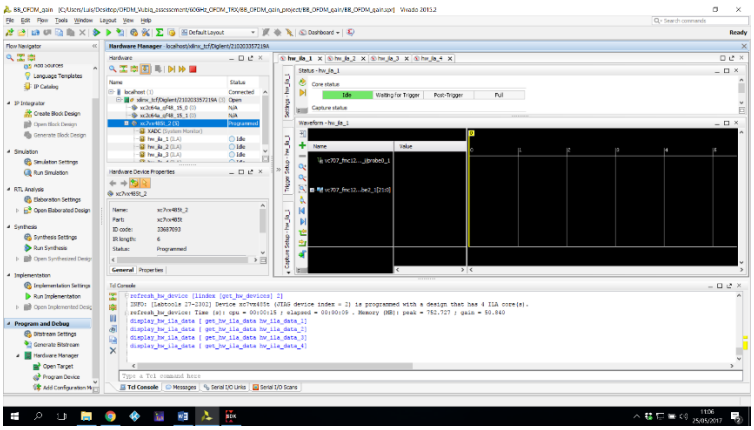


Figure 12 – ILAs at the Vivado workspace

11) After running each ILA, verify ILA1 and make sure that the synchronization signal is correct. If not, verify if the value on ILA 2 is 2.

12) If the system is not working, verify the connections and program the device again. Make sure IF is 2 when analysing ILA 1. Repeat this process until obtaining the expected results;

13) The click on **Tools → Run Tcl Script…** and select **medicoes.tcl** on the following path: *OFDM_Vubiq_assessement\3-EVM_BER*;

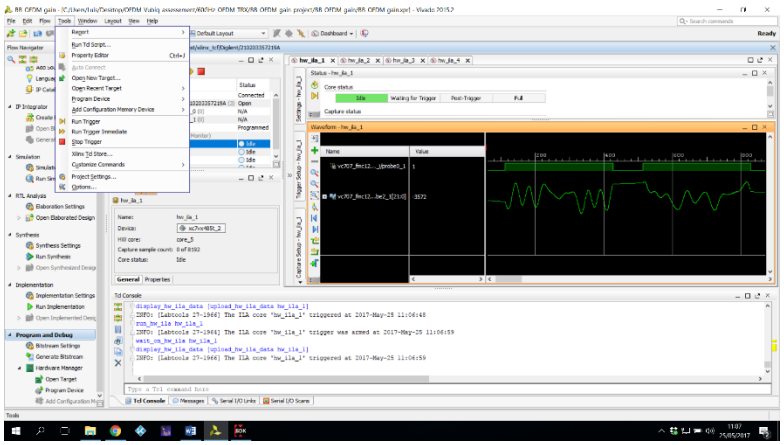


Figure 53 – Running Tcl files

14) Verify the results by running the Matlab script ***VIVADO_ILA_EVM_tester.m***, with the capture directory being *OFDM_Vubiq_assessement/3-EVM_BER/Measurements/VUBIQ_60GHz/*;

15) Repeat this test with different values of gain until its maximum value of 7, in order to achieve maximum value of Signal-to-Noise Ratio (SNR).

Second Step – IT Integration

1) Connect the signal from the transmitter box of the IT to the output of the FPGA. Then, connect the signal from the receiver box to the spectrum analyser in order to verify the correct functionality of the system;

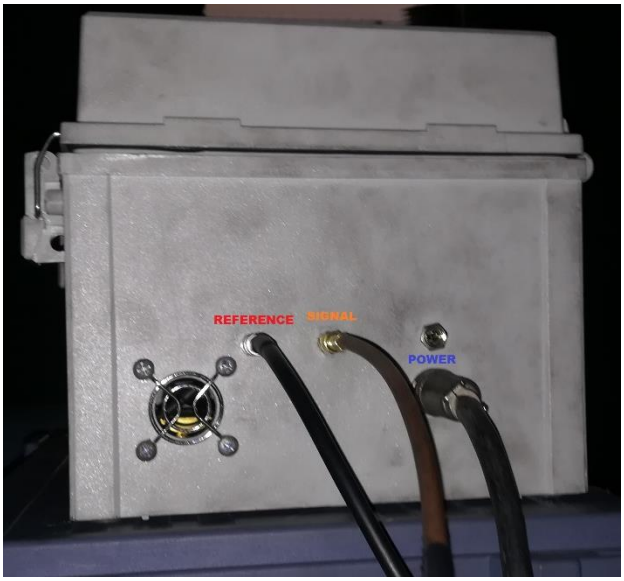


Figure 6 – HXI Cable Connections

2) Insert on the output of the rubidium signal, as seen on figure 1:

- 5 dB attenuator;
- Two low pass filters from DC to 11 MHz.

3) Connect the rubidium signal to a 0º Splitter and connect both outputs to the reference inputs of both HXI boxes. Connect the power cord to the boxes;

4) After verifying that all cables are correctly connected, power up the rubidium reference and then power up the HXI boxes with 12 V;

5) Let the signal reference stabilize for 15 minutes, warm-up time for the rubidium reference;

6) Visualize on the Spectrum Analyser the results;

7) After verifying the results, in order to improve the SNR, connect the received signal to the amplifier (ZX60-6013E+ by Mini-Circuits), by first connecting both ends and then powering it at 12V and observe the signal on the spectrum analyser;

8) Turn off the power of the amplifier and connect its output to a 0º splitter and connect one of the outputs to the spectrum analyser and the other to the FPGA ADC;

9) Power the amplifier and run the ILA and verify the signal integrity;

10) Run the tcl script and test the results on Matlab.

Appendix C

Front-end results

C.1 VUBIQ

C.1.1 Shared reference clock

IF2

Table C.1: Summary of VUBIQ results with f_c@156.25 MHz with shared clock configuration.

Gain Select	Analogue Att. [dB]	TX Input Power [dBm]	Analogue RX SNIR [dB]	$\overline{EVM}^*$ [%]	$\overline{EVM}^*$ [dB]
0	0	-25.63	26.46	32.06	-9.85
	5	-30.63	20.74	64.87	-3.66
	10	-35.63	14.80	134.60	2.61
1	0	-19.76	25.64	27.30	-11.24
	5	-24.76	28.65	55.98	-4.79
	10	-29.76	24.76	78.34	-2.06
2	0	-17.83	20.30	29.33	-10.63
	5	-22.83	27.43	31.92	-5.89
	10	-27.83	26.27	50.74	-5.89
3	0	-16.21	17.03	22.66	-12.77
	5	-21.21	22.47	23.54	-12.06
	10	-26.21	30.92	31.26	-9.80
4	0	-14.83	16.48	24.61	-12.02
	5	-19.83	21.06	25.27	-11.79
	10	-24.83	30.06	52.20	-5.11
5	0	-13.64	16.55	23.88	-12.05
	5	-18.64	18.42	26.25	-11.79
	10	-23.64	28.20	34.74	-8.70
6	0	-12.62	17.47	23.13	-12.66
	5	-17.62	18.20	28.99	-10.41
	10	-22.62	26.41	33.26	-9.11
7	0	-11.72	17.07	26.19	-11.61
	5	-16.72	**17.55**	**19.01**	**-14.34**
	10	-21.72	23.70	31.69	-9.52

* This value represents the mean of three signal captures

IF4

Table C.2: Summary of VUBIQ results with f_c@312.5 MHz with shared clock configuration.

Gain Select	Analogue Att. [dB]	TX Input Power [dBm]	Analogue RX SNIR [dB]	$\overline{EVM}^*$ [%]	$\overline{EVM}^*$ [dB]
0	0	-27,36	28.10	39.33	-7.89
	5	-32.36	21.94	66.56	-3.38
	10	-37.36	16.95	118.09	1.48
1	0	-21.59	32.84	21.70	-13.05
	5	-26.59	32.73	29.47	-10.56
	10	-31.59	26.02	50.27	-5.93
2	0	-19.68	29.68	19.44	-14.09
	5	-24.68	33.34	24.36	-12.22
	10	-29.68	28.51	38.87	-8.19
3	0	-18.11	26.52	21.83	-12.93
	5	-23.11	33.65	21.46	-13.26
	10	-28.11	30.55	32.44	-9.75
4	0	-16.76	25.47	21.10	-13.43
	5	-21.76	**32.87**	**19.32**	**-14.21**
	10	-26.76	32.42	32.78	-9.59
5	0	-15.53	24.36	22.98	-12.72
	5	-20.53	30.52	20.79	-13.52
	10	-25.53	33.34	25.81	-11.70
6	0	-14.45	23.05	29.36	-10.57
	5	-19.45	26.50	30.28	-10.31
	10	-24.45	31.95	28.17	-10.91
7	0	-13.51	23.25	28.02	-11.03
	5	-18.51	24.08	28.47	-10.87
	10	-23.51	31.21	29.87	-10.43

* This value represents the value obtained from the mean of three signal captures

IF6

Table C.3: Summary of VUBIQ results with f_c@468.75 MHz with shared clock configuration.

Gain Select	Analogue Att. [dB]	TX Input Power [dBm]	Analogue RX SNIR [dB]	$\overline{EVM}^*$ [%]	$\overline{EVM}^*$ [dB]
0	0	-27.80	31.82	48.46	-5.94
	5	-32.80	25.65	83.48	-1.04
	10	-37.80	19.07	105.81	0.67
1	0	-21.97	30.23	30.28	-10.32
	5	-26.97	32.22	36.73	-8.49
	10	-31.97	27.38	72.92	-2.25
2	0	-20.06	29.13	32.93	-9.57
	5	-25.06	32.26	32.32	-9.25
	10	-30.06	30.85	47.80	-6.06
3	0	-18.46	25.85	30.95	-10.17
	5	-23.46	31.08	30.78	-10.20
	10	-28.46	32.22	41.06	-7.62
4	0	-17.08	25.22	33.38	-9.48
	5	-22.08	29.43	34.78	-9.09
	10	-27.08	33.12	36.13	-8.81
5	0	-15.91	26.31	31.32	-10.02
	5	-20.91	28.98	31.17	-10.11
	10	-25.91	**31.39**	**28.41**	**-10.88**
6	0	-14.83	25.14	48.44	-5.68
	5	-19.83	28.20	36.65	-8.65
	10	-24.83	33.95	30.34	-10.32
7	0	-13.94	26.61	107.61	1.74
	5	-18.94	27.12	35.29	-8.95
	10	-23.94	31.43	37.36	-8.34

* This value represents the value obtained from the mean of three signal captures

C.1.2 Independent reference clock

IF4

Table C.4: Summary of VUBIQ results with f_c@312.5 MHz with independent clock configuration.

Gain Select	Analogue Att. [dB]	TX Input Power [dBm]	Analogue RX SNIR [dB]	$\overline{EVM}^*$ [%]	$\overline{EVM}^*$ [dB]
0	0	-27,36	29.04	143.44	3.75
	5	-32.36	22.45	160.64	4.51
	10	-37.36	18.21	201.21	6.26
1	0	-21.59	29.76	100.84	1.16
	5	-26.59	30.73	124.23	2.99
	10	-31.59	25.50	163.30	4.75
2	0	-19.68	27.48	97.54	0.99
	5	-24.68	32.14	120.47	2.35
	10	-29.68	27.86	102.47	1.42
3	0	-18.11	**24.17**	**63.63**	**-2.92**
	5	-23.11	31.15	83.65	-0.96
	10	-28.11	29.43	137.71	3.57
4	0	-16.76	23.00	100.02	0.71
	5	-21.76	30.26	87.77	0.12
	10	-26.76	32.23	100.59	0.98
5	0	-15.53	23.31	84.95	-0.46
	5	-20.53	28.00	85.21	-0.05
	10	-25.53	32.15	102.14	1.13
6	0	-14.45	22.92	97.24	0.77
	5	-19.45	27.30	113.84	1.942
	10	-24.45	32.70	106.82	1.38
7	0	-13.51	22.59	93.91	0.79
	5	-18.51	26.35	109.36	1.65
	10	-23.51	31.82	88.48	0.94

* This value represents the value obtained from the mean of three signal captures

C.2 IT

C.2.1 Shared reference clock

IF2

Table C.5: Summary of IT results with f_c@156.25 MHz with shared clock configuration.

Gain Select	Analogue Att. [dB]	TX Input Power [dBm]	Analogue RX SNR [dB]	Analogue RX SNIR [dB]	$\overline{EVM}^*$ [%]	$\overline{EVM}^*$ [dB]
0	0	-25.53	27.16	21.84	8.29	-21.60
	5	-30.63	23.48	21.42	13.70	-17.25
	10	-35.53	17.58	19.49	24.77	-12.13
1	0	-19.76	30.18	17.56	6.42	-23.83
	5	-24.76	30.23	23.35	7.13	-22.90
	10	-29.76	24.53	23.87	11.05	-19.28
2	0	-17.83	33.89	16.34	7.89	-22.06
	5	-22.83	31.34	22.45	6.76	-23.38
	10	-27.83	27.04	23.74	9.51	-20.40
3	0	-16.21	34.11	15.76	6.52	-23.53
	5	-21.21	33.60	21.00	6.10	-24.30
	10	-26.21	28.88	25.37	8.26	-21.63
4	0	-14.83	33.28	13.10	7.98	-22.18
	5	-19.83	33.74	19.11	6.80	-23.28
	10	-24.83	28.92	21.13	7.78	-22.15
5	0	-13.64	34.12	14.11	10.25	-19.70
	5	-18.64	34.46	18.00	7.24	-22.77
	10	-23.64	30.50	20.80	6.34	-23.88
6	0	-12.62	36.67	17.09	11.64	-18.64
	5	-17.62	34.98	17.14	7.44	-22.55
	10	-22.62	**33.47**	**27.67**	**5.90**	**-24.54**
7	0	-11.72	32.36	11.49	11.90	-18.42
	5	-16.72	35.60	16.26	7.39	-22.62
	10	-21.72	32.51	21.54	6.39	-23.86

* This value represents the value obtained from the mean of three signal captures

IF4

Table C.6: Summary of IT results with f_c@312.5 MHz with shared clock configuration.

Gain Select	**Analogue Att. [dB]**	**TX Input Power [dBm]**	**Analogue RX SNR [dB]**	**Analogue RX SNIR [dB]**	$\overline{EVM}^*$ **[%]**	$\overline{EVM}^*$ **[dB]**
0	0	-27,36	28.70	26.30	6.83	-23.30
	5	-32.36	22.90	23.90	11.56	-18.74
	10	-37.36	18.80	16.86	20.57	-13.73
1	0	-21.59	33.79	26.00	3.67	-28.72
	5	-26.59	29.78	25.58	5.75	-24.81
	10	-31.59	24.06	24.84	10.49	-19.58
2	0	-19.68	36.00	24.88	3.11	-30.13
	5	-24.68	31.00	26.04	4.87	-26.26
	10	-29.68	25.19	23.94	8.48	-21.45
3	0	-18.11	36.67	26.14	2.74	-31.21
	5	-23.11	32.42	26.18	4.40	-27.12
	10	-28.11	26.74	24.48	7.14	-22.93
4	0	-16.76	**37.81**	**25.90**	**2.35**	**-32.58**
	5	-21.76	34.00	26.00	3.44	-29.27
	10	-26.76	29.30	27.40	6.04	-24.38
5	0	-15.53	38.48	21.44	2.50	-32.36
	5	-20.53	34.22	24.46	3.08	-30.22
	10	-25.53	29.96	27.43	5.05	-25.94
6	0	-14.45	38.08	21.97	2.69	-31.36
	5	-19.45	34.00	24.91	3.07	-30.15
	10	-24.45	31.42	26.46	4.57	-26.80
7	0	-13.51	39.00	20.05	2.55	-31.87
	5	-18.51	36.02	25.24	2.58	-31.75
	10	-23.51	32.63	27.48	4.06	-27.82

* This value represents the value obtained from the mean of three signal captures

IF6

Table C.7: Summary of IT results with f_c@468.75 MHz with shared clock configuration.

Gain Select	Analogue Att. [dB]	TX Input Power [dBm]	Analogue RX SNR [dB]	Analogue RX SNIR [dB]	$\overline{EVM}^*$ [%]	$\overline{EVM}^*$ [dB]
0	0	-27.80	29.94	27.30	6.82	-23.33
	5	-32.80	22.89	21.07	11.83	-18.54
	10	-37.80	16.25	16.00	NA	NA
1	0	-21.97	34.49	26.05	3.85	-28.27
	5	-26.97	30.19	24.63	6.15	-24.22
	10	-31.97	23.61	24.54	10.56	-19.53
2	0	-20.06	33.91	26.61	3.23	-29.53
	5	-25.06	31.05	29.78	5.01	-25.80
	10	-30.06	24.15	26.38	8.43	-21.48
3	0	-18.46	38.02	26.84	2.98	-30.57
	5	-23.46	32.96	27.12	4.35	-27.23
	10	-28.46	28.36	25.24	7.18	-22.88
4	0	-17.08	39.39	23.64	2.78	-31.12
	5	-22.08	34.08	23.52	3.76	-28.49
	10	-27.08	29.50	27.60	6.17	-24.19
5	0	-15.91	**38.78**	**19.45**	**2.73**	**-31.26**
	5	-20.91	35.11	23.39	3.38	-29.41
	10	-25.91	30.00	25.89	5.49	-25.20
6	0	-14.83	39.33	26.19	2.81	-31.02
	5	-19.83	36.41	29.76	3.35	-29.48
	10	-24.83	31.18	30.72	5.01	-25.99
7	0	-13.94	41.04	18.35	3.03	-30.34
	5	-18.94	35.73	20.11	2.96	-30.56
	10	-23.94	32.38	25.18	4.49	-26.95

* This value represents the value obtained from the mean of three signal captures

C.2.2 Independent reference clock

IF2

Table C.8: Summary of IT results with f_c@156.25 MHz with independent clock configuration.

Gain Select	Analogue Att. [dB]	TX Input Power [dBm]	Analogue RX SNR [dB]	Analogue RX SNIR [dB]	$\overline{EVM}^*$ [%]	$\overline{EVM}^*$ [dB]
0	0	-25.53	31.09	29.68	5.72	-24.62
	5	-30.63	24.19	22.43	10.87	-19.01
	10	-35.53	17.09	17.72	18.02	-14.53
1	0	-19.76	38.22	22.71	4.11	-27.37
	5	-24.76	31.57	27.18	5.73	-24.55
	10	-29.76	28.07	26.81	9.36	-20.19
2	0	-17.83	36.07	17.18	4.02	-27.38
	5	-22.83	32.50	21.41	4.38	-26.80
	10	-27.83	30.64	27.21	7.78	-21.97
3	0	-16.21	38.87	22.70	4.41	-26.56
	5	-21.21	34.66	24.01	4.22	-27.22
	10	-26.21	31.00	26.64	6.37	-23.75
4	0	-14.83	37.62	16.44	4.64	-26.22
	5	-19.83	37.36	23.41	4.20	-27.18
	10	-24.83	34.70	27.36	5.63	-24.59
5	0	-13.64	37.91	15.00	4.75	-25.62
	5	-18.64	**39.22**	**22.72**	**3.88**	**-27.75**
	10	-23.64	31.52	26.84	5.19	-25.46
6	0	-12.62	35.61	13.03	5.84	-24.02
	5	-17.62	36.11	20.84	4.14	-27.09
	10	-22.62	34.02	32.32	4.70	-26.25
7	0	-11.72	40.21	21.38	6.35	-23.41
	5	-16.72	36.20	24.14	4.35	-26.73
	10	-21.72	34.33	24.52	4.11	-27.32

* This value represents the value obtained from the mean of three signal captures

IF4

Table C.9: Summary of IT results with f_c@312.5 MHz with independent clock configuration.

Gain Select	Analogue Att. [dB]	TX Input Power [dBm]	Analogue RX SNR [dB]	Analogue RX SNIR [dB]	$\overline{EVM}^*$ [%]	$\overline{EVM}^*$ [dB]
0	0	-27,36	28.27	26.19	5.40	-25.34
	5	-32.36	24.01	23.86	9.43	-20.51
	10	-37.36	18.51	20.23	16.50	-15.65
1	0	-21.59	33.45	24.58	3.01	-30.42
	5	-26.59	29.45	27.74	4.79	-26.39
	10	-31.59	25.17	24.38	8.28	-21.64
2	0	-19.68	36.43	28.30	2.62	-31.60
	5	-24.68	31.85	26.68	3.96	-28.05
	10	-29.68	26.70	25.37	6.67	-23.52
3	0	-18.11	36.57	20.87	2.30	-32.52
	5	-23.11	32.71	29.70	3.37	-29.43
	10	-28.11	28.79	27.55	5.64	-24.98
4	0	-16.76	**36.60**	**22.62**	**2.23**	**-32.99**
	5	-21.76	34.73	23.72	3.00	-30.44
	10	-26.76	30.00	28.83	4.81	-26.36
5	0	-15.53	35.96	18.83	2.31	-32.70
	5	-20.53	34.97	25.30	2.84	-30.93
	10	-25.53	29.75	26.74	4.45	-26.98
6	0	-14.45	38.51	23.15	2.26	-32.87
	5	-19.45	36.17	23.64	2.57	-31.78
	10	-24.45	30.52	24.38	3.95	-28.06
7	0	-13.51	37.15	24.73	2.37	-32.46
	5	-18.51	35.44	25.01	2.37	-32.48
	10	-23.51	33.98	29.06	3.64	-28.77

* This value represents the value obtained from the mean of three signal captures

IF6

Table C.10: Summary of IT results with f_c@468.75 MHz with independent clock configuration.

Gain Select	Analogue Att. [dB]	TX Input Power [dBm]	Analogue RX SNR [dB]	Analogue RX SNIR [dB]	$\overline{EVM}^*$ [%]	$\overline{EVM}^*$ [dB]
0	0	-27.80	29.38	27.11	5.96	-24.50
	5	-32.80	27.21	24.82	10.33	-19.72
	10	-37.80	20.54	19.84	18.70	-14.56
1	0	-21.97	36.69	23.94	3.31	-29.59
	5	-26.97	30.91	28.45	5.37	-25.40
	10	-31.97	25.90	24.48	9.20	-20.72
2	0	-20.06	38.80	32.13	2.76	-31.18
	5	-25.06	32.27	31.04	4.35	-27.23
	10	-30.06	30.73	29.39	7.40	-22.61
3	0	-18.46	38.11	28.62	2.42	-32.30
	5	-23.46	33.78	26.63	3.72	-28.58
	10	-28.46	29.91	29.01	6.20	-24.14
4	0	-17.08	39.10	28.66	2.44	-32.21
	5	-22.08	34.45	28.71	3.36	-29.46
	10	-27.08	31.37	27.02	5.45	-25.26
5	0	-15.91	**40.03**	**29.06**	**2.37**	**-32.46**
	5	-20.91	37.11	30.46	3.10	-30.15
	10	-25.91	32.47	29.67	4.85	-26.27
6	0	-14.83	40.54	19.79	2.40	-32.33
	5	-19.83	36.27	22.30	2.82	-30.99
	10	-24.83	33.68	27.52	4.39	-27.14
7	0	-13.94	40.78	26.26	2.45	-31.51
	5	-18.94	37.64	27.33	2.64	-31.57
	10	-23.94	33.85	30.56	4.05	-27.84

* This value represents the value obtained from the mean of three signal captures

Appendix D

Measurement ruler support

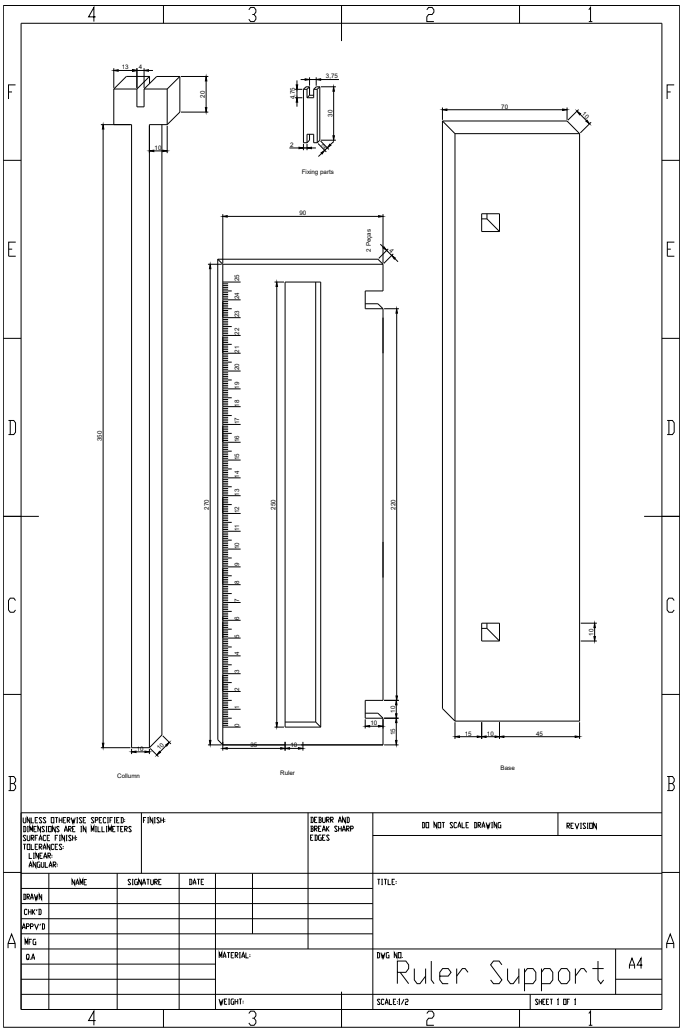


Figure D.1: Measurement ruler support measures.

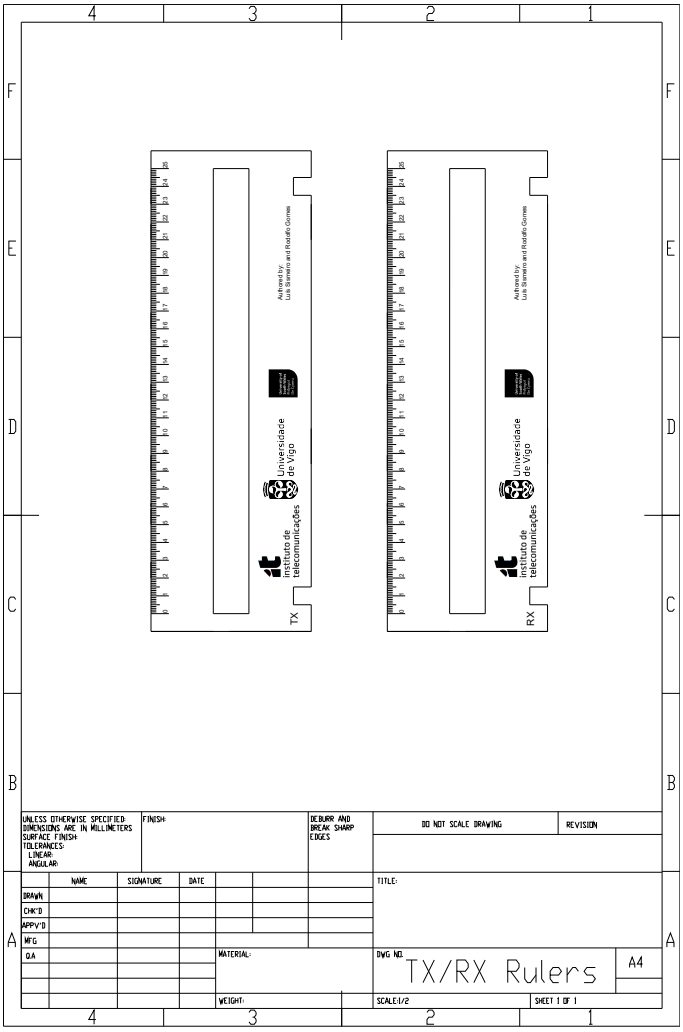
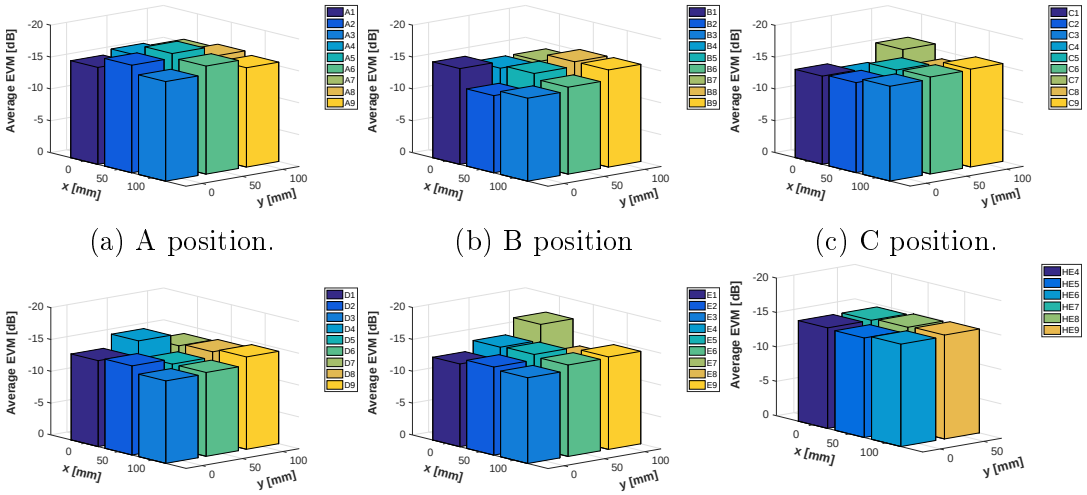


Figure D.2: TX and RX rulers with etched symbols.

Appendix E

AR Classroom results

E.1 Average EVM

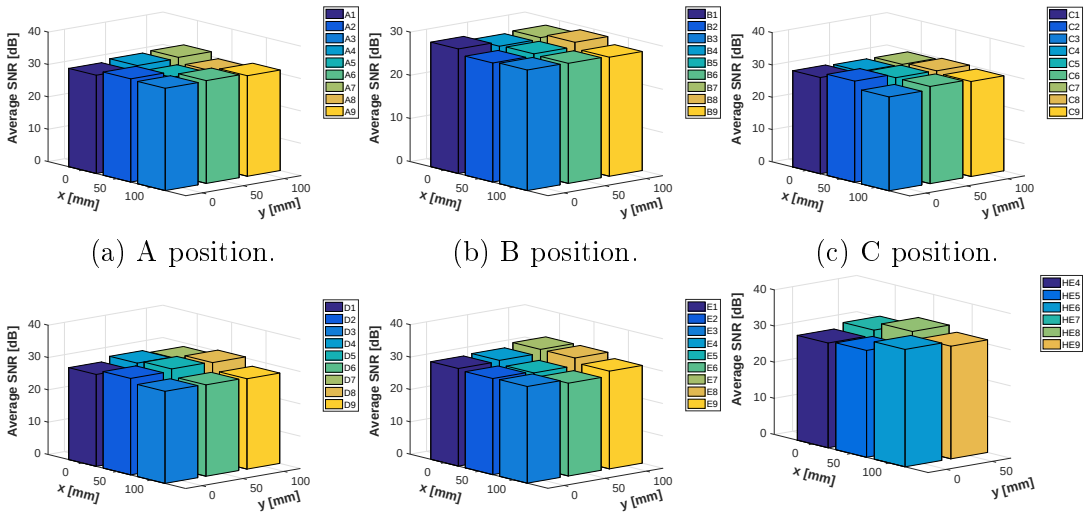


(a) A position. (b) B position (c) C position.

(d) D position. (e) E position. (f) Human effect on E position.

Figure E.1: Average EVM for all positions.

E.2 Average SNR

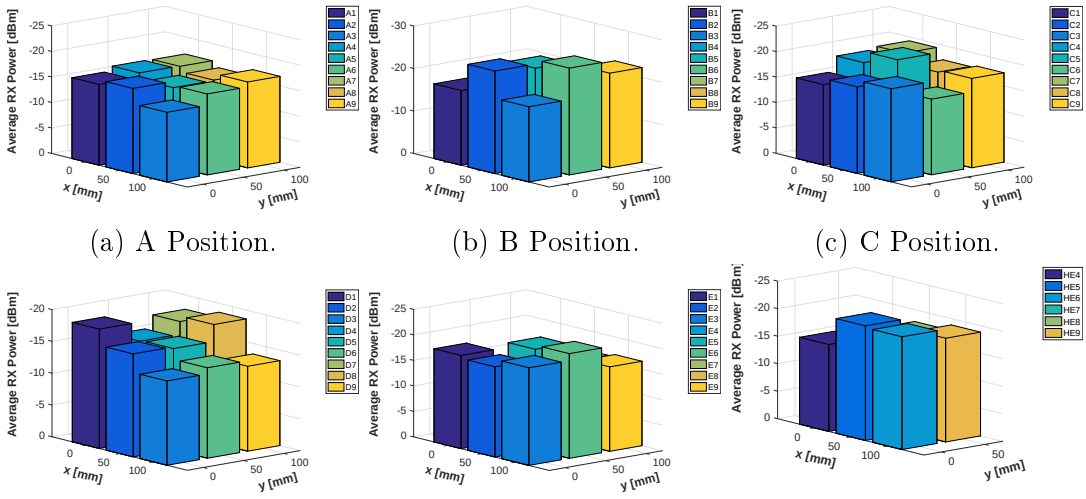


(a) A position. (b) B position. (c) C position.

(d) D position. (e) E position. (f) Human effect on E position.

Figure E.2: Average SNR for all positions.

E.3 Average RX signal power

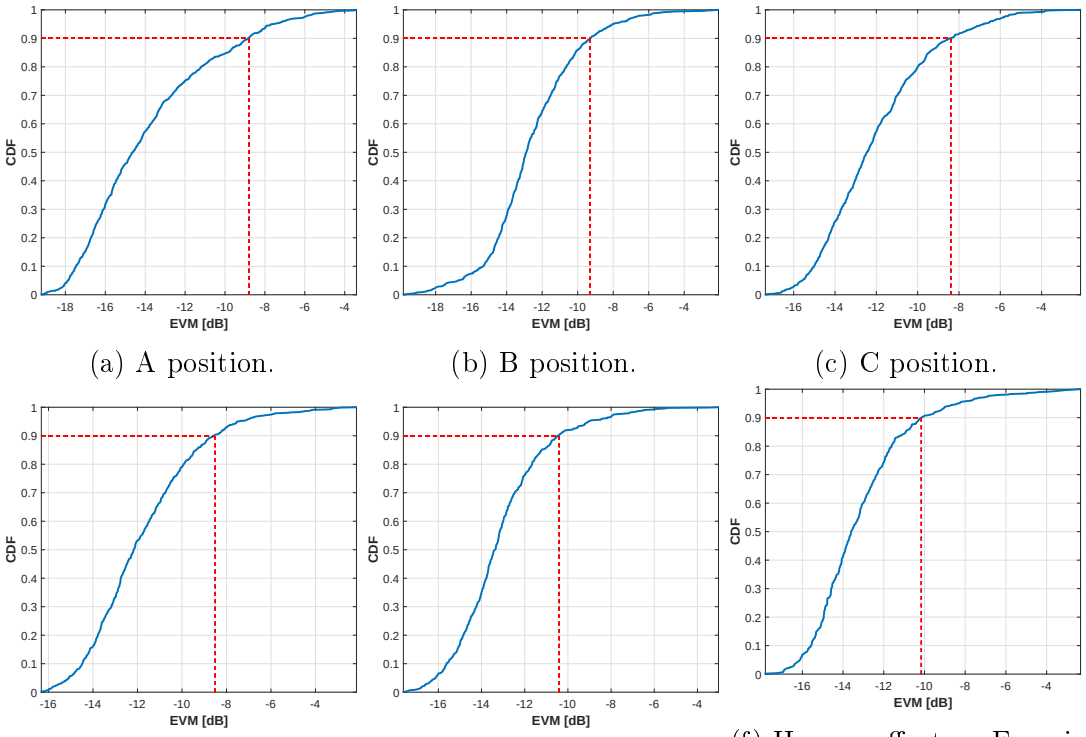


(a) A Position. (b) B Position. (c) C Position.

(d) D Position. (e) E position. (f) Human effect on E position.

Figure E.3: Average RX Power for all positions.

E.4 CDF



(a) A position. (b) B position. (c) C position.

(d) D position. (e) E position. (f) Human effect on E position.

Figure E.4: CDF for all positions.