Disruptive Future of Radar Based on All-Digital PN Signal Processing

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***Abstract*—This paper presents the first results on the design and implementation of a real-time and high resolution monostatic radar at 24 GHz, based on the sliding correlation of pseudo-noise (PN) sequences. The real-time radar, with a high time resolution better than 4ns, is used for moving target identification (MTI) in the presence of highly dense clutter, under harsh environments and severe weather conditions (fog, snow and fire smoke or plume). A radar signal processing based on all-digital PN sequences is proposed, which represents a quantum leap in radar future front-end architecture. Results obtained in a controlled environment, inside an anechoic chamber, are presented and a benchmark with a commercially-of-the-shelf solution is presented.**

***Index Terms*—STDCC, FMCW, Radar, Monostatic, PN sequences, FPGA.**

I. Introduction

Radar sensors have been deployed in the automotive industry and will foresee massive use in autonomous driving and drone based applications. In spatial reconstruction of the environment surrounding the radar becomes an important issue in many applications, including concealed-object detection and identification.

Many radar topologies that have been presented in the literature [1], mostly based on Frequency Modulated Continuous Wave (FMCW), except for some military applications, have limited performance in heavy cluttered environments. In [1], [2], Orthogonal Frequency Division Multiplexing (OFDM) is being proposed to overcome the limitations of FMCW radars, particularly by resolving several different (moving) targets in a highly dense clutter environment and interference from other radars. Quasi real-time processing demands for high computational resources typically in field-programmable gate array (FPGA) based architectures, with physical bandwidths in the order of a few GHz. These may be cumbersome if multiple radar front-ends are to be used, being limited by the analogue-to-digital converters (ADC), which typically have bandwidths below 1 GHz and prohibitive costs for mass production.

Radar signal processing based on all-digital pseudo-noise (PN) sequences represents a quantum leap in radar future front-end architecture, presenting significant advantages in terms of low baseband computational demands, yielding a plethora of opportunities for massive deployment in autonomous driving applications.

In particular, this paper presents the first trails on a Swept Time-Delay Cross-Correlator (STDCC) PN Radar at 24 GHz. The proposed radar architecture follows the STDCC principle well covered in [3]–[5] and it is sought to mitigate incumbent and mutual interference risks and interference mechanisms, given its excellent auto-correlation properties. Besides presenting radar measurement results for several case studies, obtained inside an anechoic chamber, this paper compares the performance of the proposed radar system with a FMCW commercially-of-the-shelf solution.

This paper is organised as follows: section II details the topology of the proposed radar architecture, giving particular emphasis to the radio frequency (RF) and intermediate frequency (IF) stage, including the hardware description of the main parts. Section III describes the baseband signal generation, with particular attention to the generation of the PN sequences within a FPGA environment. In section IV, the practical implementation and performance analysis of the STDCC radar are performed, considering several measurement scenarios. The performance evaluation of the proposed radar with a FMCW commercial solution is also included. Finally, the main conclusions are drawn in section V.

II. Radar Topology

This section thoroughly details the proposed system giving the necessary technical insight about the radar architecture. For instance, Fig. 1 depicts the block diagram of the radar topology. The block diagram is divided in two sub-systems, corresponding to different stages of the system's architecture, namely the RF and IF stages.

In the RF stage, a high precision Voltage Controlled Oscillator (VCO) is used to lock the phase-lock-loop (PLL) configured to output a 12.0 GHz RF signal. After appropriate signal conditioning (filtering and amplification) to suppress undesired spurious signals and adjust the power level, a frequency multiplier is employed to achieve the necessary $f_{LO} = 24$ GHz reference signal. This, in turn, is used to source both the single side band (SSB) up-converter and the IQ down-converter mixers using a 2-way power divider. Thus, the Tx mixer up-converts the base-band signal (f_{IF}) generated by an FPGA (Tx PN Sequence) in the IF stage block into a 24 GHz RF signal. Subsequently, an amplification stage is considered to increase the output power level up to the

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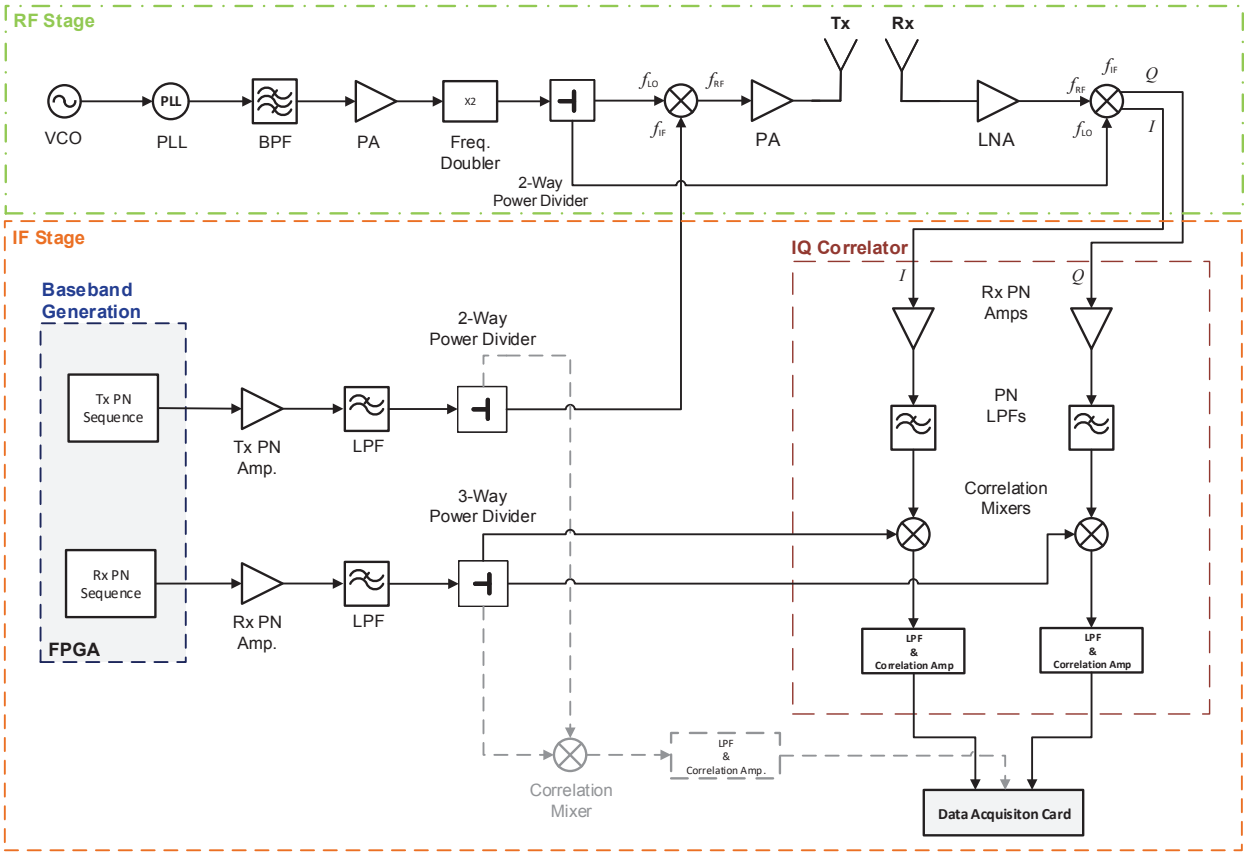


Fig. 1: Block diagram of the STDCC radar architecture.

limits of interest for the radar. On the other hand, the Rx mixer de-modulates the RF signal from the radio channel that contains radar information, into a differential signal with In-phase (I) and In-quadrature (Q) components that inputs the IQ Correlator in the IF block.

The RF stage (Fig. 1) is implemented using *X-Microwave* technology, which is a complete modular building block eco-system for microwave components that allow easy integration of RF components, aiming at fast prototyping. Two identical 20 dBi standard gain horn antennas (*Flann* 22240-20) are used side-by-side, as transmitter and receiver, distanced 1 cm apart.

In the IF Stage, a 511 bits length pseudo-noise sequence of Maximum Length Linear Shift Register (MLSR) type is generated by an FPGA at two different rates. The sequence to be transmitted over-the-air (Tx PN sequence) has a sampling rate of $f_{seqTx} = 250.1$ MHz whereas the one to be correlated in the receiver (Rx PN sequence) is decreased by 100 kHz, resulting in a sliding factor of $k = 2500$ according to (1) [3], [4]. Specifics about the baseband PN sequence generation are detailed in Section III.

$$k = \frac{f_{seqTx}}{\text{slip rate}} = \frac{f_{seqTx}}{f_{seqTx} - f_{seqRx}} = 2500 \qquad (1)$$

The differential signal that is fed into the IQ Correlator block and contains the radar information is amplified and filtered before being correlated with the Rx PN Sequence generated by the FPGA. The I and Q signals are analysed in both independent branches allowing for *Doppler* detection.

After correlation, the resulting signal is amplified and filtered, in order to be properly detected by a data acquisition (DAQ) card. To this extent, specific electronic circuitry was developed, comprising two printed-circuit boards for the amplifier and filter components, respectively. A 12-pole switch was included so that pre-defined gains can be adjusted according the specific dynamic range envisaged for a specific geometry/measurement. The gain of the post-correlation IQ signals can vary from 14 up to 19 dB, providing an appropriate level for the DAQ card input ports. As per the low-pass filter, a 7^{th} order *Chebyshev* filter, with maximum theoretical ripple of 0.01 dB, and a cut-off frequency of 200 kHz (twice the slip-rate), was implemented. This type of filter was chosen due to its steep roll-off, while minimising the pass-band ripple.

The acquisition of the correlation signals is done using a ordinary DAQ, i.e. *Picoscope* 3406-D MSO, with 4 analogue inputs of 250 MHz bandwidth, and a maximum sampling frequency of 1 GS/s and 8 bits of resolution.

In order to obtain a clear temporal reference, an optional auto-correlation stage could be included (as marked in grey

colour in Fig. 1), at the expense of using one extra correlation mixer, amplifier and filter. This is currently used in the system to reference the temporal instants and to trigger the data acquisition card for signal measurement.

III. All-Digital Baseband

The baseband block, marked with blue-dashed line in Fig. 1, is the radar sub-system responsible for generating the receiver and transmitter PN sequences. This implementation adopts 511 points maximum length real-valued bipolar PN binary sequences. The real-valued bipolar PN binary sequences open way to the use of the FPGA's unipolar digital output pins, followed by a DC removing block, to generate the analogue baseband signal, thus eliminating the need to use expensive high-speed Digital-to-Analogue (DAC) converters. The block diagram of this sub-system is depicted with more detail in Fig. 2. The baseband is composed of 3 main blocks: Clock generation, Transmitter Sequence Generation and Receiver Sequence Generation. Its outputs feed both IF stage PN amplifiers identified in Fig. 1.

The clock generation block outputs 2 digital clock signals with frequencies of 250.1 MHz and 250 MHz that feed, respectively, the transmitter sequence generation and receiver sequence generation blocks. The different frequencies fed to the transmitter and receiver sequence generation blocks are responsible for the previously identified sliding factor, crucial for the operation of the STDCC [3]–[5] algorithm. To generate two clock signals at close but different frequencies, from a single reference clock signal with a frequency of 125 MHz, two reconfigurable PLL blocks (RX Clk Generator and TX Clk Generator in Fig. 2) must be used inside the FPGA. Because this circuit was implemented in a Xilinx Kintex-7 FPGA KC705 Evaluation Kit [6], the PLL blocks are implemented with 2 Xilinx's mixed-mode clock managers (MMCM) [7]. The receiver MMCM receives the 125 MHz clock signal and is configured to output 2 clock signals with different frequencies: the 250 MHz clock signal that will drive the receiver sequence generation block, and a 13.864818 MHz clock signal that will drive the transmitter MMCM. The transmitter MMCM is configured to output the 250.1 MHz clock signal that will drive the transmitter sequence generation block.

The transmitter and receiver sequence generation blocks are identical. The only difference is the frequency of the clock signal that drives them. Each sequence generation block is composed of a binary counter and a ROM. The 9-bit binary counter counts from 0 to 510, sequentially addressing the 512-words, single bit-depth ROM. The ROM holds the unipolar version of PN binary sequence adopted in the implementation. The outputs of both ROMs are routed to 2 digital output pins, configured with the highest slew rate and drive strength.

IV. Practical Implementation and Performance Analysis

A. Experimental Setup

In order to assess the performance of the proposed radar, the setup of Fig. 3 was assembled inside the anechoic chamber

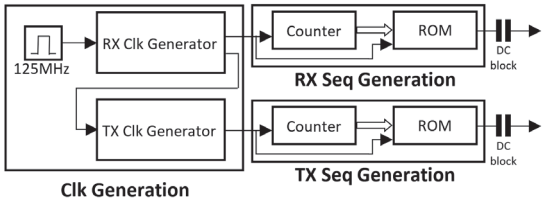


Fig. 2: STDCC radar baseband.

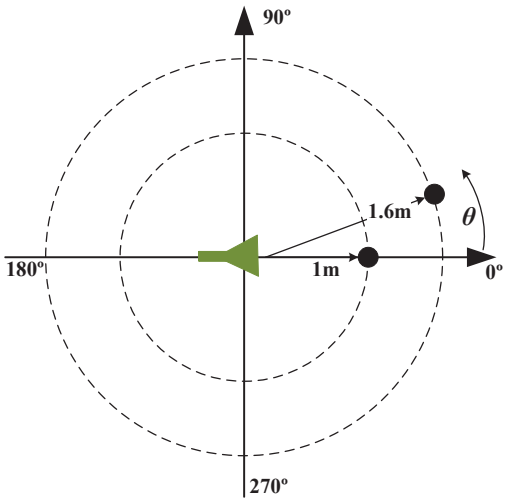


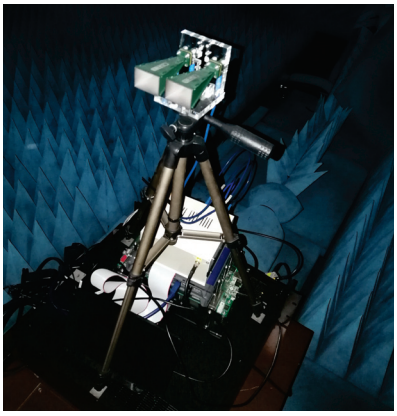
Fig. 3: Radar benchmark setup.

to reduce the multipath effects and avoid possible external RF interferences. The radar prototype was placed, according to Fig. 4a, at the centre of the 6 m by 5 m chamber, on top of a motorised turntable, that enables 360° rotation in the azimuth plane (represented herein by θ) with 0.5° resolution. Several case studies have been considered by placing metallic poles with 6 cm of diameter and 2 meters height, at the vicinity of the radar. The poles were distributed inside the anechoic chamber according to geometry depicted in Fig. 3. Radar measurements for distance and angular dependences, using both STDCC and FMCW radars, have been performed in the following order:

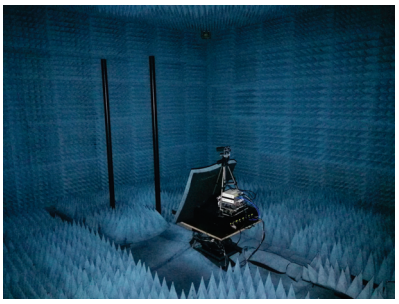
1) A single metallic pole, placed 1 m apart of the proposed radar aperture, at boresight direction ($\theta = 0^\circ$);
2) Two metallic poles, one placed at 1 m at boresight direction and the other at 1.6m steered off 10° from the boresight direction ($\theta = 10^\circ$).

For both geometries, the radar system under test was made to rotate 360° with a 0.5° steps increment. It is also important to mention that for every step taken, 20 radar acquisitions have been measured and then averaged (Power Delay Profile) to obtain a plan position indicator (PPI) and assess the target identification performance. As stated, the STDCC radar target identification performance was assessed with one and two metallic poles and later compared with an off-the-shelf FMCW

commercial solution (Distance2Go, from Infineon).



(a)



(b)

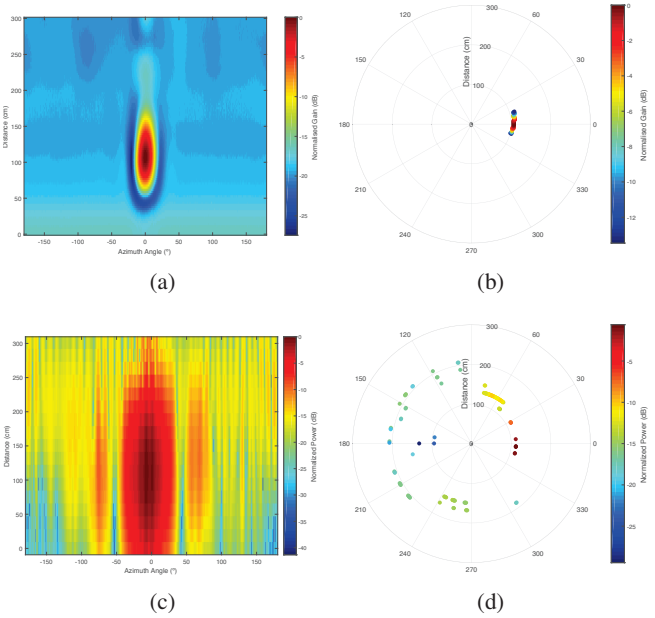
Fig. 4: (a) Photography of the STDCC radar prototype, (b) Two-pole experimental setup assembled inside the anechoic chamber.

In the first scenario, the proposed radar was placed in the middle of an anechoic chamber on top of the turntable with one pole 1m apart and at bore-sight (0°). As explained in the previous section, both I and Q signals were considered for correlation and their results have been squared and summed together which, when plotted, yield the PDP result per angle. To better illustrate the radar performance, such values are plotted in two graph types: waterfall and polar plots, as depicted in Figs. 5a and 5b, respectively. While the waterfall graph presents the measured averaged PDP, for every angular step in the azimuth plane, displaying the radar distance in the y-axis and the azimuth angle in the x-axis, the polar plot shows the detected peaks, at each scanned angle, after running a simple peak-detection algorithm.

B. Experimental Results

To evaluate the performance of both STDCC and FMCW radars, several measurements have been considered. The respective results are presented and discussed in this section side-by-side for a more convenient analysis. From Fig. 5a, it can be concluded that the STDCC radar is accurately detecting a peak at 1 m distance at 0°, corresponding to the correct pole location inside the anechoic chamber. In fact, this can be confirmed in the plot of Fig. 5b, that clearly identifies an object at 1m away from the radar at boresight direction to the object. However, it is worth to mention that the gradient variation of colours around the detected object, in Fig. 5a, is associated to the antennae radiation pattern discrimination that exhibits an half-power beam-width of around 23°, in both azimuth and elevation planes, at the considered frequency.

On the other hand, with the commercially available radar, it is also possible to detect the same pole, as depicted in the plan position indicator of Fig. 5c. From the experimental data, an object is detected at 0° and a peak value at 1.1 m. Interestingly, several artefacts, albeit being 5-10 dB below the main contribution, are also observed almost in any direction. Due to this fact, the polar plot of Fig. 5d depicts false positives, since other peaks rather than the main contribution have also been detected by the peak-detection algorithm.



(a) (b)

(c) (d)

Fig. 5: Experimental results for one-pole scenario: (a, c) waterfall PPI plots and (b, d) polar PPI plots for, the STDCC and FMCW radars, respectively.

Furthermore, when conducting the second set of experiments, i.e. maintaining the 1 m distance pole and adding a second pole at 1.6 m deviated 10° in azimuth (according to the diagram of Fig. 3), it is possible to observe that both radars are detecting the artificial targets. From the experimental results of Fig. 6, both STDCC and FMCW radars are still able to detect the metallic pole placed 1 m distance, with the STDCC radar (Fig. 6a) presenting a slight advantage with a greater measurement accuracy, when compared with the FMCW one (Fig. 6c). However, when the second pole is added to the scenario, it can be seen from Fig. 6c that the commercial solution fails to resolve such object. Although a slight increase in power at the region of $\theta = 10^\circ, d = 1.5$ m is noticed, it is not possible to clearly distinguish between the two objects. In fact, it seems the second pole is masked by the effect caused by the pole placed

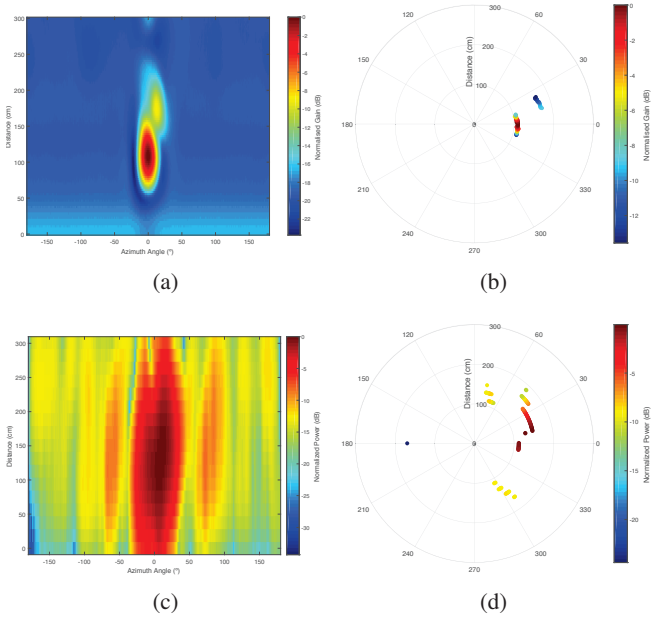


Fig. 6: Experimental results for two-pole scenario: (a, c) waterfall PPI plots and (b, d) polar PPI plots, for the STDCC and FMCW radars, respectively.

at 1 m apart. Similarly to the first measurement (Fig. 5c), many artefacts are also observed in the 360° scan with amplitudes 5-10 dB below the main reflections.

In this particular case, the STDCC radar really show its merits and stands out from its counterpart, since it is able to clearly detect and distinguish both metallic poles (Figs. 6a and 6b), at the correct locations, *i.e.* first pole at $\theta = 0°, d = 1$m and second pole at $\theta = 10°, d = 1.6m$. In fact, these results have been consistent throughout a series of repeated measurements, and a maximum range discrepancy of only 9 cm have been detected between experimental radar data and effective physical distance. This error is acceptable, as it falls within the spatial precision associated with the bandwidth used in the proposed radar. The signal level difference of about 7-9 dB observed in Fig. 6a is due to the excess path loss corresponding to distance of flight between poles (i.e. 1.2 m), in addition reflection loss introduced by the second pole (i.e around 2 dB).

From the results above, it is possible to state that the proposed system is capable to detect closely space objects in the limit of the radar spatial resolution and thus presenting a remarkable performance over the tested commercial solution.

V. Conclusions

Understanding of existing and emerging radar waveforms based on STDCC and their limit factors on both time/spatial resolutions and range have been consolidated and validated against measurements. A radar signal processing based on all-digital PN sequences has been proposed, representing a quantum leap in radar future front-end architecture. The future radar technology, and hence the disruptive future, should be capable to operate in multi-user operation in several deployment environments using orthogonalisation signals between different radars (users). This is sought to be accomplished by taking advantages of the orthogonality of the proposed technique based on STDCC, as in typical radio channel sounders, in which the implementation and acquisition of baseband signals (PN) is assumed to be all-digital. And thus, to reduce production costs and make it a good candidate for mass-production. Finally, the potential of multi-PN transmission for direction-of-arrival estimation and radar imaging, is well underway.

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