Dynamic jitter accumulation in clock repeaters considering power and ground noise correlations

Conference Paper · May 2011

DOI: 10.1109/ISCAS.2011.5938128 · Source: DBLP

2 authors:

Monica Figueiredo
Polytechnic Institute of Leiria
53 PUBLICATIONS **190** CITATIONS

SEE PROFILE

Rui L. Aguiar
University of Aveiro
565 PUBLICATIONS **4,879** CITATIONS

SEE PROFILE

Dynamic Jitter Accumulation in Clock Repeaters Considering Power and Ground Noise Correlations

Mónica Figueiredo* and Rui L. Aguiar†
*School of Technology and Management, Polytechnic Institute of Leiria, P-2411-901, Leiria, Portugal
†Department of Electronics, Telecomunications and Informatics, Aveiro University, P-3810-193, Aveiro, Portugal
*† Institute of Telecomunications, Aveiro site, P-3810-193, Aveiro, Portugal
monica.figueiredo@ipleiria.pt , ruilaa@ua.pt

***Abstract*—This paper discusses the mechanism behind dynamic jitter accumulation in clock repeaters, considering the impact of power supply noise correlations. We show that differential and common mode noise have a different impact on jitter accumulation, depending on correlations between cascaded repeater stages. We also propose a simple accumulation model that can be used to replace time-consuming transient noise simulations. Besides providing an useful insight regarding the impact of noise correlations on jitter accumulation, the model's accuracy is shown to be within 10% of SPICE results.**

***Index Terms*—Jitter, Power Supply Noise, Clock Repeaters.**

I. Introduction

Most dynamic jitter models are based on the assumption that power variations are mirrored in the ground distribution network [1], [2]. This is true when all the devices share the same power and ground voltages, and is typical in wire-bonded dies. However, trends in device and packaging technology have changed this traditional assumption and differential mode noise (DMN) can no longer be generally considered dominant. It has been shown in [3] that common mode noise (CMN) has a significant impact on delay variability and thus, should not be neglected when analyzing jitter in clock distribution networks. However, their analytical approach fails to address the impact of correlation between noise sources in adjacent repeaters.

In this paper we investigate the impact of noise correlations on clock jitter accumulation. The popular statistical accumulation model states that the variance of the sum of uncorrelated random variables is the sum of their variances and the standard deviation of the sum of totally correlated random variables is the sum of their standard deviation. Although this model is commonly used to describe jitter accumulation [4]–[6], it disregards the impact of input noise on the repeater's response to its own power supply noise (PSN) sources.

To solve this issue, we propose a modified statistical accumulation model for dynamic jitter. It can be used to predict jitter accumulation bounds with higher accuracy than the conventional statistical approach, with a residual computational cost. Also, it provides a better insight regarding the complementary mechanisms of jitter generation and accumulation, as well as regarding the impact of noise correlations. We will show that if noise sources are totally correlated in cascaded repeaters, DMN jitter accumulates much faster than CMN jitter. On the contrary, DMN jitter accumulates slower if noise sources are weakly correlated. This insight and the ability to accurately predict jitter bounds in cascaded repeaters can be useful to promote floorplan-based power and clock distribution design in order to minimize jitter accumulation. This can be particularly effective in bump-bonded and low inductance package styles, where DMN is not dominant and cascaded clock repeaters may experience uncorrelated PSN contributions.

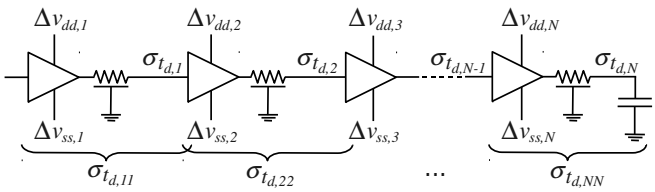

Fig. 1. Cascaded CDCs and their output jitter.

The rest of this paper is organized as follows. In section II, we explain the mechanism behind jitter accumulation in clock repeaters and propose a modified statistical model, considering noise correlations. Section III evaluates the proposed model accuracy and discusses the impact of noise correlations on jitter accumulation. Conclusions are given in section IV.

II. Dynamic Jitter Accumulation Model

A. Jitter in Cascaded Repeaters

In cascaded repeaters, jitter associated to a clock path depends on jitter generated by each clock distribution cell (CDC) on that path. CDCs are usually designed to exhibit similar input and output transition times, so a given clock path can be represented by a cascade of balanced CDCs (with similar effective fanouts). In Fig. 1, we represent such a general clock path with N equivalent CDCs affected by PSN sources. Here, $\sigma_{t_{d,i}}$ is the total jitter observed at the output of cell i, which is different from the jitter generated in cell i ($\sigma_{t_{d,ii}}$), due to jitter amplification and accumulation.

To explain the physical mechanism behind jitter amplification, we present here the results of a simple experiment with three cascaded CDCs. We varied the supply and ground levels on the first cell and compared the waveforms along that line (v_{ni}) with the waveforms of a reference line (v_{ri}), with nominal supply and ground levels. Fig. 2 shows the waveforms

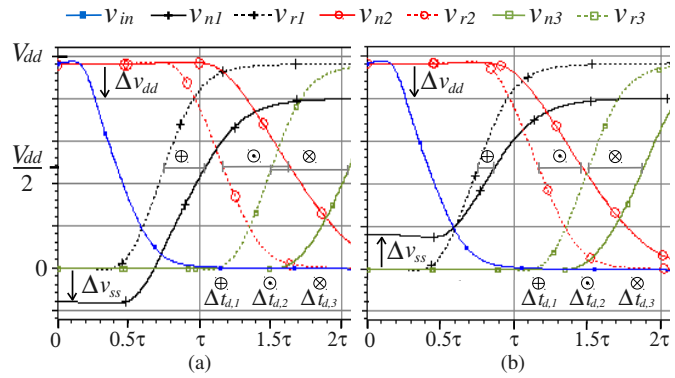

Fig. 2. Waveforms of a reference CDC line (v_{ri}) and a CDC line affected with PSN in the first cell only (v_{ni}) for: a) CMN; b) DMN.

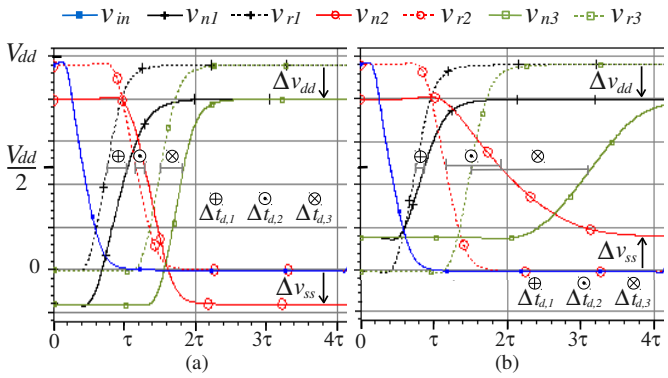

Fig. 3. Waveforms of a reference CDC line (v_{ri}) and a CDC line with the same PSN sources in all cells (v_{ni}) for: a) CMN; b) DMN.

for CMN and DMN, where Δt_{di} is the instantaneous delay error observed at the output of cell i. Note that absolute jitter is by definition the standard deviation of Δt_{di} [4].

The graphics show that for both CMN and DMN, the instantaneous delay error introduced by the first cell is transfered to the second cell with gain. This gain results from the fact that the second cell's input voltage is different from its supply voltage, which affects its response to the input transition. After the second cell, the delay error does not increase because there is no further influence of PSN sources (applied to the first cell only). The gain for uncorrelated PSN sources (g^u) has shown to depend on the relative position between the noisy CDC and the observed cell, and to be higher for DMN than for CMN. It has also been shown to depend on the CDC design parameters, as will be discussed latter in this paper.

A second experiment was performed to observe jitter gain when CDCs have totally correlated PSN sources. We used the same repeater line, but now all cells share the same power and ground levels. The resulting waveforms are shown in Fig. 3. We can see that the instantaneous delay error measured at the second cell is not twice the error measured in the first cell, as we would expect in a cascade of identical cells with correlated noise sources. For CMN, the amplification gain is even negative (attenuation), which almost mitigates jitter accumulation. This negative effect of CMN in cascaded inverters has also been observed in [3]. On the contrary, DMN causes a significant jitter amplification as all contributions have a positive effect on jitter accumulation. The gain for correlated sources (g^c) is thus different from g^u, although it also depends on the noise mode and CDC design parameters.

B. Bounds for Jitter Accumulation

If PSN sources are uncorrelated in each CDC, we can use the superposition principle and an amplification gain parameter to estimate jitter along the line, as shown in (1). The gain elements define a lower triangular matrix $[g^u]$ with ${g_{ij}}^u = 0$, for $j > i$ and ${g_{ij}}^u = 1$, for $j = i$. Each element ${g_{ij}}^u$ is the gain applicable to jitter generated in cell j in order to obtain its contribution to jitter in cell i. Note that we sum jitter variances because jitter contributions from uncorrelated sources are independent random variables (the superscript u stands for uncorrelated noise sources). To obtain the individual estimates $\sigma_{t_{d,ii}}$, we can use Monte Carlo simulation results for voltage variations [6], transient noise simulations [7] or a scalable jitter model like the one proposed in [8].

$$[{\sigma^2_{t_{d,i}}}^u]_{N\times 1} = [{g^2}^u]_{N\times N} \cdot [{\sigma^2_{t_{d,ii}}}^u]_{N\times 1} \quad (1)$$

If PSN sources are totally correlated, we cannot use the superposition principle. In this case, the dynamic jitter after N cells depends on the sum of individual standard deviations and on the gain for totally correlated sources. In (2) we show the expression to compute dynamic jitter at the output of cell k in a cascade of N cells. The superscript c indicates the assumption of correlated PSN sources.

$$[{\sigma_{t_{d,i}}}^c]_{N\times 1} = [g^c]_{N\times 1} \cdot \sum_{i=1}^{k} {\sigma_{t_{d,ii}}}^c \quad (2)$$

C. Jitter Amplification Gain Characterization

In a general clock path, the amplification gain depends on many different design and noise parameters, and is associated with the repeater's non-linear behavior during the signal transition. Thus, it is not straightforward to derive an accurate analytical model for $[g^u]$ and $[g^c]$. Instead, we propose an heuristic method based on the characterization of a reference repeater line with $N = 5$ similar CDCs. Screening experiments revealed that this is a sufficient number of cells to provide an accurate characterization.

For uncorrelated PSN sources, the amplification gain can be obtained with transient noise simulations with PSN applied to the first cell only. This can be done because g^u dependsonly on the relative position between the noisy CDC and the observed cell. We used MATLAB to generate a set of power and ground noise samples (with the same standard deviation σ_{v_n}), which were imported into SPECTRE as piece-wise linear files in CMN and DMN configurations. Simulations were repeated for different noise modes, noise variances and CDC design parameters. The relevant design parameters in this line are the CDC's fanout ratio ($r_f = C_{out}/C_{in}$) and resistance ratio

($r_r = R_{int}/R_{rep}$). Here, R_{int} is the interconnect resistance, R_{rep} is the repeater's ON resistance, C_{in} is its input capacitance, and C_{out} is its output capacitance, which includes both the interconnect (C_{int}) and load capacitances (C_L).

Simulation results were then used to obtain the gain elements (${g_{ij}}^u$), computed as the ratio between jitter measured at the output of cell i and jitter generated in the first cell ($j = 1$), as shown in (3). For correlated PSN sources, the amplification gain elements (${g_i}^c$) can be obtained with a similar procedure, but with the same PSN sources applied to all CDCs in the line. They are computed as the ratio between the jitter measured at the output of each cell and the total expected jitter at that node. In this case, the expectable jitter at the output of cell N is just N times the jitter observed at the first cell (4).

$$ {g_{ij}}^u = {\sigma_{t_{d,i}}}^u / {\sigma_{t_{d,jj}}}^u \ , \ i = 1, ...N \ , \ j = 1 \tag{3} $$

$$ {g_i}^c = {\sigma_{t_{d,i}}}^c / \left(i \cdot {\sigma_{t_{d,1}}}^c\right) \ , \ i = 1, ..., N \tag{4} $$

Simulation data can then be arranged in look-up tables or fitted into polynomial expressions. For uncorrelated PSN sources, the gain elements depend on the noise mode, the noise standard deviation as a percentage of the supply voltage ($\nu_n = \sigma_{v_n}/V_{dd}$), the fanout ratio r_f, the resistance ratio r_r and the relative position between the observed cell and the noisy cell ($M = i - j$). If PSN sources are totally correlated, the gain elements have the same dependencies but now the relative position M is replaced by the number of cascaded cells (N). This is summarized in (5) and (6), for uncorrelated and totally correlated noise sources, respectively. Here, ${f_d}^u$, ${f_c}^u$, ${f_d}^c$ and ${f_c}^c$, are polynomial expressions that fit characterization data.

$$ {g_{ij}}^u = \begin{cases} 1 \ , & i = j \\ {f_d}^u(M, \nu_n, r_f, r_r) \ , & i > j \wedge DMN \\ {f_c}^u(M, \nu_n, r_f, r_r) \ , & i > j \wedge CMN \\ 0 \ , & i < j \end{cases} \tag{5} $$

$$ {g_i}^c = \begin{cases} 1 \ , & i = j \\ {f_d}^c(N, \nu_n, r_f, r_r) \ , & i = 2, ..., N \wedge DMN \\ {f_c}^c(N, \nu_n, r_f, r_r) \ , & i = 2, ..., N \wedge CMN \end{cases} \tag{6} $$

In Fig. 4 we present ${g_{k1}}^u$ and ${g_k}^c$ results, with $k = 1, ..., 5$, obtained for a 90nm inverter repeater. For uncorrelated noise sources, jitter amplification is shown to be almost constant after the second cell and higher for DMN than for CMN. The most relevant design parameter is shown to be r_r, which significantly reduces jitter accumulation. This means that interconnect resistance is beneficial for jitter accumulation when PSN sources are uncorrelated. When noise sources are correlated, r_r also has a beneficial impact on DMN jitter accumulation but the most relevant parameter is shown to be noise amplitude (ν_n). On the contrary, jitter gain for CMN is shown to be very low ($<< 1$) and depend almost exclusively on the number of cascaded cells.

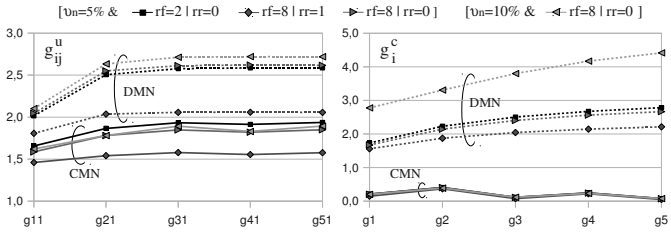

Fig. 4. Jitter gain for different design parameters and noise correlations.

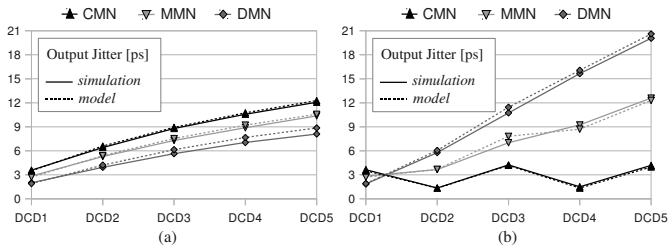

Fig. 5. Jitter model evaluation for CMN, DMN and MMN: a) uncorrelated; and b) correlated noise sources.

III. Accumulation Model Evaluation

A. Model Accuracy

Model results are compared with simulation data, using a two stage symmetric H-tree implemented in a 90nm technology. Each clock path has five inverter-based CDCs with $r_f = 4$. We considered a uniform load distribution and geometric wire sizing. Jitter accumulation along the tree was then evaluated with transient simulations, using low-frequency noise sources with different modes, amplitudes and correlations along the clock paths. Low-frequency means that the noise cut-off frequency is lower than the clock frequency.

In Fig. 5 we compare simulation results with model predictions, for uncorrelated and totally correlated PSN sources. Each plot shows the results for CMN, DMN and mixed-mode noise (MMN) sources, with $\nu_n = 3\%$. MMN sources follow independent random sequences, which results in 50% CMN and 50% DMN in each CDC. In Fig. 6 we graphically represent the model accuracy with x-y plots. The x-axis corresponds to model predictions while the y-axis corresponds to simulation results. We can see that jitter is well estimated, with most points falling above the 45 degrees line. The model error, calculated as a percentage of the simulation results, is shown to be inferior to 10%. Note that individual jitter estimates were obtained using a scalable jitter model based in [8], which also contributes to this error.

Our model was also evaluated for trees designed with variable interconnect parameters (C_{int} and R_{int}), wire sizing techniques (geometric or uniform) and chip size. However, it is not practical to graphically represent the results for all of these experiments. We prefer to quantify the model accuracy with the plots shown in Fig. 7. Jitter is shown to be well estimated, with most points falling on the 45 degrees line. Again, the model error is inferior to 10% in all the experiments.

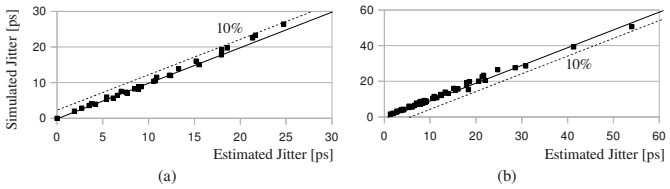

Fig. 6. Model accuracy: a) uncorrelated; b) correlated noise sources.

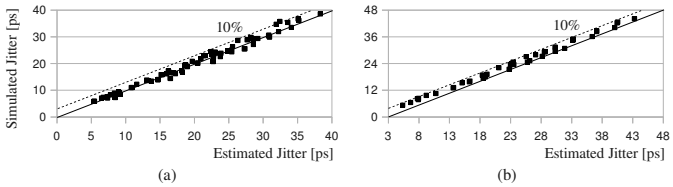

Fig. 7. Jitter model accuracy for different interconnect parameters, wire sizing techniques, chip sizes and: a) 2 stages ($N = 5$); and b) 3 stages ($N = 7$).

B. Discussion on Jitter Accumulation

At this point, it is interesting to discuss the implications of noise correlations on dynamic jitter accumulation. Circuits with wire-bonded packages usually have symmetric power and ground noise variations (dominant DMN). We have shown in Fig. 5 that DMN is beneficial for jitter accumulation only if noise sources in adjacent repeaters are uncorrelated. However, most PSN in wire-bonded packages is low-frequency and highly spatially correlated [9]. In this case, jitter accumulation can only be reduced if noise sources can be decorrelated, using dithering or similar techniques.

For bump-bonded and low inductance packages, DMN is dominant only if cascaded repeaters share the same local power distribution parasitics (when repeaters lie in the same power block). In this case, noise sources are probably also highly correlated and jitter accumulates fast. On the contrary, if clock repeaters are placed in different power blocks, DMN may no longer be dominant. This is beneficial for jitter accumulation if noise sources are correlated in adjacent repeaters, but detrimental if they are independent. In this scenario (repeaters placed in different power blocks), noise sources are not expected to be totally correlated and we cannot take fully advantage of the beneficial impact of CMN. Nevertheless, we believe that this approach can result in a positive net effect because the beneficial impact of CMN for correlated sources is by far more significant than its detrimental effect for uncorrelated sources. Also, this difference becomes more pronounced with the number of cascaded repeaters.

C. Comparison with Statistical Model

Simulation results shown in Fig. 5 are here compared with results obtained with the conventional statistical accumulation (SA) model. In Fig. 8, we show the SA model error computed as the difference between SA model predictions ($\sigma_{t_{d,i|SA}}$) and simulation results ($\sigma_{t_{d,i}}$), as a percentage of simulation results ($\epsilon = (\sigma_{t_{d,i|SA}} - \sigma_{t_{d,i}})/\sigma_{t_{d,i}}$). We can see that the SA model fails to predict dynamic jitter accumulation in most situations. When noise sources are uncorrelated, the statistical model (sum of variances) follows the same trends shown by simulation results, but underestimates jitter with an error around -40% after only five clock repeaters. When noise sources are totally correlated, the statistical model (sum of standard deviations) provides even worse predictions. For CMN, jitter is considered to accumulate very fast disregarding the positive effect of CMN in cascaded inverters. In this case, the error is big and non-monotonic. The error is also significant for DMN and MMN, with $\epsilon_{dmn} \approx -50\%$ and $\epsilon_{mmn} \approx 15\%$.

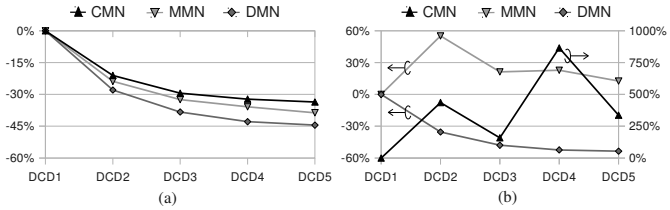

Fig. 8. SA model error: a) uncorrelated; b) correlated noise sources.

IV. Conclusion

In this paper we analyze jitter accumulation in clock repeaters. We propose a simple and accurate model to predict dynamic jitter accumulation bounds, considering noise correlations between power and ground distribution networks, and between adjacent repeaters. Simulation results have shown that the proposed model provides much more accurate predictions than the conventional statistical model, which disregard the impact of input PSN. The presented analysis, where jitter generation and accumulation are seen as complementary mechanisms, may also be helpful to grasp the importance of noise correlations on dynamic jitter accumulation.

References

[1] M. Saint-Laurent and M. Swaminathan, "Impact of power-supply noise on timing in high-frequency microprocessors," *Advanced Packaging, IEEE Transactions on*, vol. 27, no. 1, pp. 135–144, Feb. 2004.

[2] J. Jang, O. Franza, and W. Burleson, "Period jitter estimation in global clock trees," in *Proc. 12th IEEE Workshop on Signal Propagation on Interconnects, SPI 2008*, May. 2008, pp. 1–4.

[3] L. Chen, M. Marek-Sadowska, and F. Brewer, "Buffer delay change in the presence of power and ground noise," *Very Large Scale Integration (VLSI) Systems, IEEE Trans. on*, vol. 11, no. 3, pp. 461–473, Jun. 2003.

[4] T. Weigandt, "Low-timing-jitter design techniques for delay cell based vcos and frequency synthesizers," Ph.D. dissertation, University of California, Berkeley, 1998.

[5] T. Xanthopoulos, *Clocking in Modern VLSI Systems*. Springer Publishing Company, Incorporated, 2009, ch. 2.

[6] V. Wason, R. Murgai, and W. Walker, "An efficient uncertainty- and skew-aware methodology for clock tree synthesis and analysis," in *Proc. 20th International Conference on VLSI Design*, Jan. 2007, pp. 271–277.

[7] M. Figueiredo and R. Aguiar, "Time precision comparison of digitally controlled delay elements," in *Proc. IEEE Int. Symposium on Circuits and Systems, ISCAS 2009*, May. 2009, pp. 2745–2748.

[8] ——, "Clock repeater characterization for jitter-aware clock tree synthesis," in *Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation*, ser. Lecture Notes in Computer Science, J. Monteiro and R. van Leuken, Eds. Springer Berlin / Heidelberg, 2010, vol. 5953, pp. 46–55.

[9] I. Kantorovich and C. Houghton, "Maximum tolerable power supply noise for data-clock synchronization," in *Proc. 2006 IEEE Electrical Performance of Electronic Packaging*, Oct. 2006, pp. 167–170.