Clock Repeater Characterization for Jitter-Aware Clock Tree Synthesis

Monica Figueiredo[Λ] and Rui L. Aguiar[Σ]

Instituto Politécnico de Leiria, Escola Superior de Tecnologia e Gestão[Λ]
Universidade de Aveiro, Dpt. Electrónica e Telecomunicações[Σ]
Instituto de Telecomunicações[ΛΣ]
Leiria, Aveiro, Portugal
monicaf@estg.ipleiria.pt,ruilaa@ua.pt

Abstract. This paper presents a simple jitter model for clock repeaters. The model is scalable and technology independent, which makes it suitable for integration in current clock tree synthesis algorithms. It is based on the timing characterization of a reference inverter, which can be performed for different process corners to account for process variability. Simulation results show that the model is accurate to within 10% for the most common inverter and NAND based repeaters.

Key words: Jitter Model, Clock Repeaters, CTS

1 Introduction

Clock Tree Synthesis (CTS) is a layout technique to optimally distribute repeaters along the path between clock sources and receivers with the minimum skew in clock arrival times. Skew depends on many different parameters associated with the clock distribution network: the number of stages; the repeater's size and locations; the on-chip spacial and temporal load distribution; and the interconnect structure. Various approaches to CTS have been proposed to minimize skew such as symmetric and asymmetric trees [1], optimal repeater insertion and repeater/wire sizing schemes [2] or tunable repeaters [3].

Timing uncertainties also depend on process, voltage and temperature (PVT) variations, physical and circuit noise sources. In [4], clock skew is evaluated under several variability models while a statistical methodology to compute time uncertainties under the impact of PVT, power supply noise (PSN) and crosstalk is presented in [5]. Other works focus on PSN induced jitter estimation and minimization. In [6], jitter estimation in clock trees is based on a recursive analytical expression considering sinusoidal PSN, while [7] presents analytical expressions for buffer delay variation. Jitter minimization is usually accomplished with clock buffer polarity assignment techniques [8], with intentional clock skew introduction or clock frequency modulation [9]. Due to the increasing relevance of jitter in high-speed digital designs, it is our belief that it should be accounted for as early as possible in the design flow. It is thus desirable to have jitter minimization during CTS through a proper choice of repeaters, their size and location.

In this paper we present a model for jitter generated in clock repeaters based on a reference inverter timing characterization, which can be performed for different process corners to account for process variability. This pretends to be a simple and efficient tool to enable the introduction of jitter-awareness in CTS algorithms, concerning jitter generated in repeaters. Other jitter sources and accumulation models should be considered in future work to allow system level jitter modeling. The characterization and model generation flow is schematically represented in Fig. 1. The model can be based on delay parameters usually available on technology library files, but a more extensive timing characterization can also be done specifically for this purpose. Although the characterization has to be done for each technology, the model itself is technology independent and allows jitter estimation for any clock repeater, given its specific design parameters and a particular PSN model. The PSN model should be selected according to the circuit's design, as will be explained in section 2.3.

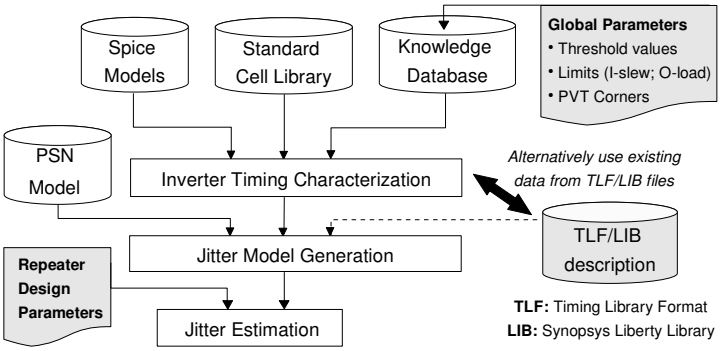

Fig. 1. Characterization and model generation flow.

During CTS, repeaters are optimally sized and separated to minimize the interconnect delay and guarantee sharp clock edges at receivers. However this typically requires an increased number of large buffers, which may draw huge current from power/ground network and incur in PSN, which is a main jitter source. To identify current-hungry repeaters during CTS, we propose the usage of a simple current model based on the popular triangular approximation. Peak current information can then be used as an input parameter during the CTS decision process to minimize auto-induced jitter in clock repeaters.

The paper is organized as follows. In section 2 we describe the clock distribution cell and the noise sources that affect its precision. After, we present the inverter and buffer characterization methodology and the proposed jitter model. Model predictions are compared with simulation results in a 180nm technology, for these inverter based clock repeaters. The model applicability to other repeaters is presented in section 3. Section 4 discusses the usage of current models for auto-induced jitter prediction and conclusions are given in section 5.

2 Jitter Model

2.1 Clock Distribution Cell

The most common topology of clock distribution networks is the clock tree with repeaters. Symmetric H-trees were typically adopted in high performance designs for global clock distribution due to their intrinsic low skew characteristics. However, balanced trees with repeaters are usually preferred in the presence of obstructions or non-uniform load distribution, which is the most common situation in present designs. In both structures, a clock distribution cell is defined from the input of one clock driver to the input of the next clock driver, which includes the repeater, the interconnects and load. In this work we will only focus on the repeater's jitter model, with interconnects and load modeled as a single effective load capacitance [10].

For a given number of cascaded clock distribution cells, wire interconnects and total driving capacitance, the repeaters' sizes determine the cell's delay and transition times. These choices will also determine the jitter associated with each cell because jitter is known to directly depend on transition times [11]. Clock repeaters are usually designed to produce equal rise and fall times, propagating a nearly constant clock pulse width throughout the distribution network, but other options may contribute to minimize power consumption [12]. Regarding architecture, the most common clock repeaters are buffers and inverters. Other increasingly popular options include tristate or AND-type repeaters for clock gating, and tunable delay repeaters (TDR) to adjust delay variations.

2.2 Inverter Jitter Model

We propose a model to estimate jitter generated in clock inverters ($\hat{\Delta t}_{d,inv}$) based on a reference jitter value ($\Delta t_{d,ref}$) and scalable correction factors ($\Upsilon(r_j)$) (1). The correction factors vary according to the inverter's size ($r_s = s/s_{ref}$), fanout ($r_f = C_{out}/C_{in}$) and on the ratio between input and output transition times ($r_{io} = t_{in}/t_{out}$). The mean rising/falling transition time should be used even if the inverter is not balanced, because each distributed clock edge will be equally affected by rising and falling inverters in a repeater chain.

$$\hat{\Delta t}_{d,inv} = \Delta t_{d,ref} \cdot \prod_j \Upsilon(r_j) \ , \quad j \in \{s, f, io\}. \tag{1}$$

The first step to obtain the correction factors is to select a reference inverter, with a reference fanout and input transition time. Any drive strength can be chosen for this purpose but simpler factors result if we choose the smaller inverter available in the clock repeater's library, with $r_f = r_{io} = 1$. The second step is to characterize the inverter's output transition time (t_o) and delay (t_d) for different sizes, loads and input transition times. The timing data is usually already available in the technology library file, but can also be easily obtained from simulation. The third step is to curve/surface fit the data to analytically model t_o and t_d with r_s, r_f and r_{io} as arguments.

Having done this, empirical correction factors can be obtained from the ratios shown in (2). There are two output transition time ratios ($r_{to,s}$ and $r_{to,io}$) and one delay time ratio ($r_{td,f}$). The ratios $r_{to,s} = t_{o,r_s}/t_{o,ref}$ and $r_{td,f} = t_{d,r_f}/t_{d,ref}$ are obtained with $r_{io} = r_f = 1$, while the ratio $r_{to,io} = t_{o,r_{io}}/t_{o,ref}$ is obtained for different r_f factors and $r_s = 1$. The quadratic jitter dependence on $r_{to,io}$ results from the known significant impact of the input transition time on propagation delay. Hence, care must be taken when characterizing the reference inverter for different input transition times. It is advisable that similar inverters are used as driving gates and the slew rate measured at $30-90\%$ V_{dd} rising ($10-70\%$ V_{dd} falling), as usually recommended.

$$\Upsilon(r_s) = \sqrt{r_{to,s}} \; ; \; \Upsilon(r_f) = r_{td,f} \; ; \; \Upsilon(r_{io}) = (r_{to,io})^2 \tag{2}$$

2.3 Buffer Jitter Model

Clock buffers are just a cascade of two inverters (with eventually different sizes). Their output jitter variance depends on the jitter introduced by each inverter and the correlations among the noise sources involved [7]. So, we can use the inverter's model to estimate jitter in clock buffers as long as adequate design parameters are inferred for each inverter and the noise sources are characterized. In (3) and (4) we present the inverter's design parameters based on the buffer's parameters $\{\Gamma_n; r_s; r_f; r_{io}\}$, where Γ_n is the buffer's tapering factor. Some of these parameters are given as approximations, but the exact values can be obtained through simulation (for a given technology) if higher accuracy is desired.

$$Inv_1 : \{r_{s,1} = r_s/\Gamma_n; \; r_{f,1} \approx \Gamma_n; \; r_{io,1} \approx r_{io}\sqrt{r_f/\Gamma_n^2}\} \tag{3}$$

$$Inv_2 : \{r_{s,2} = r_s; \; r_{f,2} = r_f/\Gamma_n; \; r_{io,2} \approx \sqrt{\Gamma_n^2/r_f}\} \tag{4}$$

In a clock repeater the input waveform depends on noise introduced by the previous repeater, which is usually placed in a distant location, probably with independent power/ground rails. So, the input transition levels can be considerd independent of buffer's PSN levels, as shown in Fig. 2. In this scenario, the buffer's output jitter is given by the sum of the individual inverter's standard deviations, based on the inverter's reference jitter (rms), multiplied by a PSN correction factor (Υ_{psn}), as shown in (5).

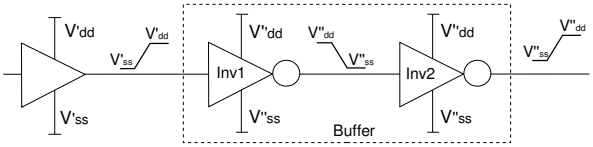

Fig. 2. PSN sources in cascaded buffer repeaters.

$$\Delta\hat{t}_{d,buf} = \left(\Delta\hat{t}_{d,inv1} + \Delta\hat{t}_{d,inv2}\right) \cdot \Upsilon_{psn}. \quad (5)$$

This factor varies between 0 and 2 for different design parameters and PSN correlations inside the buffer cell. When power and ground rails have dominant common mode noise (CMN), positive jitter generated in one inverter is canceled by negative jitter generated in the other and $\Upsilon_{psn} \approx 0$, as CMN has opposite effects on rising and falling transitions. On the other hand, if differential mode noise (DMN) is dominant, jitter can be as high as 2 times the sum of jitter (rms) in the individual inverters ($\Upsilon_{psn} \approx 2$), as those values depend on $\Delta t_{d,ref}$, obtained with independent PSN sources (with 50% CMN and 50% DMN).

2.4 Model Evaluation

To evaluate the proposed jitter model we used time domain noise simulation with independent power/ground noise sources, characterized by a PSN correction factor $\Upsilon_{psn} = 0.29$. Table 1 and 2 shows the model error for inverters and buffers with different r_s, r_f, r_{io} and Γ_n ratios. The inverter's jitter predictions have less than 5% error while the buffer's model error is inferior to 10%. Higher accuracy could be obtained if we have used an exact characterization of each inverter's design parameters, instead of the approximate values defined in (3) and (4).

Table 1. Inverter Model Evaluation

Parameters			$(\Delta\hat{t}_{d,inv}/\Delta t_{d,ref})$		
r_s	r_f	r_{io}	sim	model	error
40	2	1.0	1.436	1.441	0.32%
100	4	1.0	2.390	2.374	0.66%
200	6	1.0	3.477	3.387	2.59%
6	4	0.8	2.138	2.156	0.88%
60	3	1.4	2.304	2.250	2.32%
30	2	1.6	1.924	1.877	2.45%

Table 2. Buffer Model Evaluation

Parameters				$(\Delta\hat{t}_{d,buf}/\Delta t_{d,ref})$		
r_s	r_f	r_{io}	Γ_n	sim	model	error
40	16	1.0	4	1.834	1.852	0.99%
80	12	1.0	4	1.609	1.705	5.93%
3	6	1.0	3	1.260	1.313	4.22%
100	6	0.8	2	1.255	1.146	8.68%
160	16	0.6	4	1.604	1.732	7.97%
50	6	1.2	5	1.454	1.560	7.33%

To characterize the PSN sources we evaluated the ratio between the buffer's and the sum of the inverter's output jitter. This ratio is plotted in Fig. 3, for $\Gamma_n = 1$ and $\Gamma_n = 4$, using independent, filtered white gaussian noise sources in power and ground rails. Above each plot we present the mean and standard deviation of the measured values. The ratio is shown to weakly depend on the buffer's design parameters, except for the case when r_{io} is small, which is not a common situation in clock repeaters. The ratio does not depend on r_s, at least for common buffer sizes.

The data presented in Fig. 3 could be obtained for every possible Γ_n and arranged in a lookup table to fully characterize the impact of this particular set of

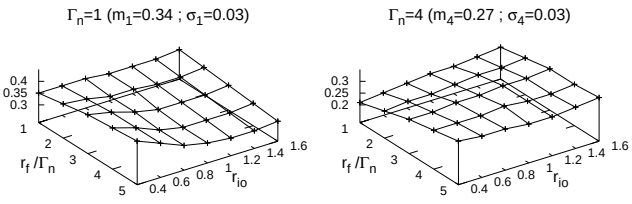

Fig. 3. Ratio between the buffer's and the total inverter's output jitter.

PSN sources. However, this procedure would take intensive simulation to obtain data for every possible combination of design parameters, which is contrary to our goal of obtaining a simple jitter model. Because the ratio is shown to be almost independent of the buffer's design, we can use a simpler model based on a reference value obtained for a buffer with middle range design parameters. For a buffer with $\{\Gamma_n = 3; r_f = 3; r_{io} = 1\}$ we have obtained $\Upsilon_{psn} = 0.29$.

Other noise sources would result in a different Υ_{psn} model. In Fig. 4, we compare the Υ_{psn} factor for independent PSN sources with the factors obtained for dominant CMN and DMN sources. These plots show that Υ_{psn} is almost independent of the buffer's design parameters for independent noise sources because the CMN and DMN variations cancel out. If this is not the case, Υ_{psn} should be modeled as a linear function of the buffer's design parameters, especially if DMN sources are predominant. The predominant noise mode should be inferred from the power supply network design or from previous designs.

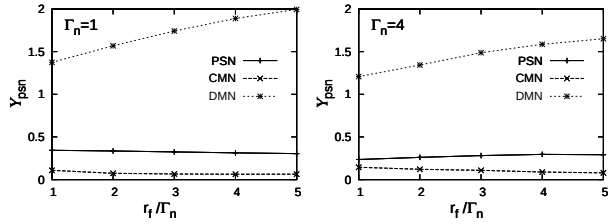

Fig. 4. Buffer's Υ_{psn} for different noise modes and design parameters.

3 Applicability to Other Repeaters

3.1 Asymmetrical Inverters

In circuits with single-edge triggered flip-flops, it is possible to design asymmetrical inverters that focus the majority of their drive current on the critical clock edge. These are called single edge clock (SEC) inverters [13]. When used

as clock repeaters, SEC inverters are designed to have the same size ($W_p + W_n$) as balanced symmetrical inverters so they can be used as drop-in replacements, although their $\beta = W_p/W_n$ is varied. When strong pull-up (Inv_r) and strong pull-down (Inv_f) SEC inverters are cascaded in a clock distribution network, the critical and the neglected clock edges are distributed through virtually different networks. The critical (neglected) clock edge will see bigger (smaller) transistors than in the case of symmetrical inverters, but with the same capacitive load. In (6) we present the relation between the size of PMOS and NMOS transistors in SEC inverters, compared to symmetrical inverters.

$$W_{n,sec} = \frac{1+\beta}{1+\beta_{sec}} \cdot W_n \ ; \ W_{p,sec} = \frac{(1+\beta)\beta_{sec}}{(1+\beta_{sec})\beta} \cdot W_p \ . \tag{6}$$

Because each repeater is equivalent to two virtual ones, they must have two associated jitter models: one related to the inverter seen by the critical clock edge (fast inverter) and another for the inverter seen by the neglected edge (slow inverter). The critical clock edge sees a fast inverter because the load is smaller than what would be expected in a symmetrical inverter with that transistor's size. Likewise, the neglected clock edge sees a slow inverter because its load is bigger than expected. As long as equivalent fanouts are defined for these virtual inverters, the data obtained for the reference symmetrical inverter can be used to estimate their output jitter.

By definition, the load capacitance of a SEC inverter is the same as its equivalent symmetrical inverter $C_L = r_f(\beta + 1)C_{gn} = C_{L,sec}$, where C_{gn} is the NMOS gate capacitance. On the other hand, the repeater's output transition times $t_{LH,sec}$ and $t_{HL,sec}$ depend on the output load and the transistor's resistance ($R_{p,sec}$ and $R_{n,sec}$). Using the Elmore delay model, the Inv_r transition times can be expressed as shown in (7), where t_{LH} and t_{HL} are the transition times of equivalent inverters with r_f=1.

$$t_{LH,sec} = t_{LH}\frac{W_p}{W_{p,sec}} \cdot r_f \ \wedge \ t_{HL,sec} = t_{HL}\frac{W_n}{W_{n,sec}} \cdot r_f \ . \tag{7}$$

The factors affecting the reference transition times can also be seen as factors affecting the virtual inverter's load. Using these relations, the equivalent r_f ratio for the fast and slow inverters in a Inv_r are defined in (8). The same could be done to obtain the equivalent r_f ratios for the virtual inverters in a Inv_f.

$$r_{f,slow} = \frac{W_n}{W_{n,sec}} \cdot r_f \ ; \ r_{f,fast} = \frac{W_p}{W_{p,sec}} \cdot r_f \ . \tag{8}$$

In table 3 we show the model error for the fast and slow virtual inverters in a strong pull-up SEC inverter (Inv_r), for which $\beta_{sec} > \beta_{ref}$. Results show the applicability of the symmetrical inverter model to SEC inverters, with an error below 10% for different combinations in design parameters.

Table 3. SEC Jitter Model Evaluation

Inv_r SEC Inverter					$\Delta\hat{t}_{d,sec}/\Delta t_{d,ref})$
r_s	r_f	r_{io}	β_{sec}/β	Type	error
4	1	1.2	2.00	slow	8.10%
10	4	1.0	1.66	slow	1.07%
12	2	0.8	1.33	slow	0.45%
4	1	1.2	2.00	fast	6.73%
10	4	1.0	1.66	fast	4.32%
12	2	0.8	1.33	fast	2.15%

Table 4. NANDs Jitter Model Evaluation

NAND gate			$\Delta\hat{t}_{d,nand}/\Delta t_{d,ref})$
r_s	r_f	r_{io}	error
10	3	1.0	1.36%
40	3	1.0	0.86%
60	2	1.0	0.33%
100	4	0.8	1.68%
160	4	1.2	2.48%
20	1	1.4	0.51%

3.2 Tunable Delay Repeaters

Various implementations of TDRs exist in literature, for different purposes and applications. Repeater chains feeding a multiplexer can be used as TDRs but have three significant drawbacks when used in clock distribution networks: 1) jitter accumulation along the chain; 2) high minimum tuning delay; and 3) high power overhead due to continuous switching of the repeaters along the chain. In this field, the most common solution is to digitally control the speed of a typical buffer or inverter. There are three basic techniques to accomplish that: the variable resistor inverter (VRI), the current-starved inverter (CSI) and the shunt-capacitor inverter (SCI). The first two can be used to design asymmetric TDRs while the last technique is intrinsically symmetric.

The inverter/buffer jitter model proposed in this paper can be directly applied to TDRs. Asymmetrical VRIs and CSIs behave like SEC inverters, with different rise and fall transition times. In symmetrical VRIs and SCIs, both transitions have the same controlled delay and thus, behave similarly to balanced inverters. Jitter generated in these repeaters depends on their transition time and so, a TDR corresponds to as many virtual inverters as the possible delay increments, each of which has its own jitter model. To reduce the complexity of such approach, the model can be applied only to the virtual inverter with the higher introduced delay (worst case jitter), the lower introduced delay (worst case current consumption), or a combination of both.

3.3 NAND Gates

NAND gates are commonly used as clock gating repeaters, available with symmetrical transition times and variable drive strengths. It is known that a two-input NAND gate with the same driving strength of a CMOS inverter has a higher input capacitance and self load factor. So, we can not use the reference inverter's data to estimate jitter on NAND gate repeaters. However, the model proposed in (1) and (2) can still be applied as long as a reference NAND gate is characterized. Simulation results with a reference NAND gate with the same

driving strength as the reference inverter are shown in Table 4. The model shows an error inferior to 5% for different NAND designs.

4 Auto-Induced Jitter

Although PSN is usually considered an external noise source, the switching activity of large clock repeaters can itself generate sharp potential drops/surges. To reduce the on-chip PSN generation, there are some techniques which apply to clock repeaters. It is possible to reduce the repeater's peak current reducing its drive strength or increasing the turn-on time, at the cost of increased delay and noise sensitivity. Low swing drive circuits have been proposed to reduce power consumption and noise generation but other considerations such as complexity, reliability and performance have limited their popularity. By delaying the transitions in some buffers, using intentional skews, clock modulation or multiphase clock distribution, the current consumption is more evenly distributed in time, giving lower PSN generation. Because these techniques can effectively reduce PSN generation and limit self-induced jitter in clock repeaters, the current consumption waveform should be considered part of their jitter characterization.

Several current consumption models have been proposed in literature. However, for the purpose of identifying current-hungry clock repeaters during CTS, high accuracy in waveform prediction is not essential. We propose a simple scalable model based in [14], but with lower data storage requirements. Our approach is based on the symmetrical triangular approximation for the inverter's current waveform, which can be characterized by its peak current (I_p), duration (D_p) and position (P_p). The current model depends these three values, obtained for the reference inverter, to which are applied size, fanout and input transition time correction factors (9).

$$\{\hat{I}_p; \hat{D}_p; \hat{P}_p\} = \{I_p; D_p; P_p\}_{ref} \cdot \prod_j \Upsilon(r_j) \ , \quad j \in \{s, f, io\}. \tag{9}$$

The correction factors are shown in Table 5. There are two output transition time ratios ($r_{to,s}$ and $r_{to,io}$) and three current ratios ($r_{Ip,f}$, $r_{Dp,f}$ and $r_{Pp,f}$). The transition time ratios are the same as the ones used in the jitter model, while the current ratios ($r_{k_{p,f}} = k_{p,r_f}/k_{p,ref}$, with $k \in \{I, D, P\}$) must be obtained during the characterization phase, with $r_{io} = r_s = 1$. Simulations have shown this model to have an accuracy within 10%, which is considered to be sufficient for this purpose.

5 Conclusion

In this paper we proposed a simple model for PSN induced jitter in the most common clock repeaters. It is based on the timing and current waveform characterization of a reference repeater. The model is scalable, technology independent, and can account for process variability if the inverter is characterized in different

Table 5. Current Model Correction Factors

	$\hat{I}_p$	$\hat{D}_p$	$\hat{P}_p$
$\Upsilon(r_s)$	$r_s/\sqrt{r_{to,s}}$	$\sqrt{r_{to,s}}$	$\sqrt{r_{to,s}}$
$\Upsilon(r_f)$	$r_{Ip,f}$	$r_{Dp,f}$	$r_{Pp,f}$
$\Upsilon(r_{io})$	$1/r_{to,io}$	$r_{to,io}$	r_{io}

process corners. For clock buffers, the model requires an additional characterization of the expected PSN in both ground and power rails. Results have shown that it has an accuracy within 10% for inverter and NAND based repeaters, which fulfills our goal to develop a simple yet efficient tool to introduce jitter awareness in CTS tools, with minimal changes and complexity increase.

References

1. Friedman, E.G., "Clock distribution networks in synchronous digital integrated circuits," Proceedings of the IEEE , vol.89, no.5, pp.665-692, May 2001.
2. Jeng-Liang Tsai et al., "Zero skew clock-tree optimization with buffer insertion/sizing and wire sizing," IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, vol.23, no.4, pp. 565-572, April 2004.
3. Chakraborty, A. et al., "Dynamic Thermal Clock Skew Compensation Using Tunable Delay Buffers," IEEE Trans. on VLSI Systems, vol.16, pp. 639-649, June 2008.
4. Hashimoto, M. et al., "Statistical analysis of clock skew variation in H-tree structure," 6th Int. Symp. Qual. Elect. Design, pp. 402-407, March 2005.
5. Wason, V. et al., "An Efficient Uncertainty- and Skew-aware Methodology for Clock Tree Synthesis and Analysis," Int. Conf. on VLSI Design, pp. 271-277, Jan. 2007.
6. Jinwook Jang et al., "Period Jitter Estimation in Global Clock Trees," 12th IEEE Workshop on Signal Propagation on Interconnects, pp.1-4, 12-15 May 2008.
7. Chen, L.H. et al, "Buffer delay change in the presence of power and ground noise," IEEE Trans. on VLSI Systems, vol.11, no.3, pp. 461-473, June 2003.
8. Samanta, R. et al., "Clock Buffer Polarity Assignment for Power Noise Reduction," IEEE/ACM Int. Conf. on Computer-Aided Design, pp.558-562, 5-9 Nov. 2006.
9. M. Badaroglu et al., "Digital ground bounce reduction by supply current shaping and clock frequency modulation," IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, vol. 24, no. 1, pp. 65-76, Jan. 2005.
10. O'Brien, P.R.; Savarino, T.L., "Modeling the driving-point characteristic of resistive interconnect for accurate delay estimation," IEEE Int. Conf. on Computer-Aided Design - ICCAD-89, pp.512-515, Nov 1989.
11. Hajimiri S. L. A., Lee T. H., "Jitter and phase noise in ring oscillators", IEEE JSSC, vol. 34, pp. 790804, Jun. 1999.
12. Tawfik, S. A., Kursun, V., "Buffer Insertion and Sizing in Clock Distribution Networks with Gradual Transition Time Relaxation for Reduced Power Consumption", IEEE Int. Conf. on Electronics, Circuits and Systems, pp. 845-848, Dec. 2007.
13. Mueller, J.; Saleh, R., "Single Edge Clock Distribution for Improved Latency, Skew, and Jitter Performance," 21st Int. Conf. VLSI Design, pp.214-219, 4-8 Jan. 2008.
14. Osorio, J.F. et al. "Extraction of Circuit Elements for Macromodel-Based Estimation of Substrate Noise", XX Conf. Design Circ. Integrated Syst., pp. 1-6, 2005.