Projeto

Mestrado em Engenharia Electrotecnica – Energia e Automação

Reconfigurable Power Quality Analyser

João Fernando de Aguiar Fazendeiro

Leiria, *março* de *2015*

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Projeto de Mestrado realizada sob a orientação da Doutora Mónica Jorge Carvalho de Figueiredo, Professora da Escola Superior de Tecnologia e Gestão do Instituto Politécnico de Leiria e coorientação do Eng° Filipe Tadeu Oliveira, Professor da Escola Superior de Tecnologia e Gestão do Instituto Politécnico de Leiria.

Leiria, *março* de *2015*

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Dedication

I dedicate this work to Our Lord and Our Lady of Fátima, to my two nephews Thomas and Daniel, my godson Rui Pedro and my parents.

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Acknowledgements

I would like to thank my employer Santuário de Nossa Senhora do Rosário de Fátima for having given me the opportunity to do this Master's Diploma, my parents for their wisdom and support and my professors for their motivation, patience and support in the difficult moments. A special thank you goes to my employer's administrator Padre Cristiano Saraiva and Rector Padre Carlos Cabecinhas for their understanding and flexibility in allowing me time for this project, to my colleagues and friends from ESTG.

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Abstract

Electronic power supplies are found in almost all electrical equipment. They are sensitive to power quality disturbances but they themselves are causers of interference. This becomes more prominent with their wider use which means that these disturbances have a tendency to aggravate in future. One of the results will be that additional losses will occur and end-users will also be penalised for it by paying more. There is a need to revert this tendency also in an effort to help lower pollution. Another consequence of disturbances is the added difficulty that power grid operators will have to maintain the network stable. Everyone would therefore benefit from more efficient electricity consumption. A power quality disturbance can be measured with a power quality analyser to help the technician find its cause. This is the first step to finding a solution to resolve the disturbance.

The objective of this project was to implement digital signal processing algorithms on a FPGA for the analysis of power quality disturbances. The motive for choosing the FPGA was that it allowed a processor, used for lower demanding processing tasks, and dedicated hardware, used for time-critical operations, to be integrated into a single integrated circuit. The implementation of these algorithms in dedicated hardware permitted obtaining high-resolution measurements and the exploitation of parallelism to increase the quantity of information available to the user. The FPGA is a versatile component, ideal to implement the reconfigurable power quality analyser that is upgradable in future.

The project resulted in the successful measurement of the fundamental frequency and the magnitude of the signal at the input. The device was able to detect and measure harmonic and inter-harmonic components. Positive and negative peak values were measured and the root mean square value both for full-cycle and half-cycle were calculated making stationary signal variation evaluation possible. Time aggregation of values was also done. The generation of an internal signal made it possible for the comparison with the input signal, resulting in event isolation for further verification and classification by the controller.

Keywords: disturbances, FPGA, monitor, power, quality, variations

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Resumo

Fontes de alimentação eletrónicas encontram-se em quase todos os equipamentos elétricos. São sensíveis a perturbações da qualidade de energia mas são elas próprias fonte de interferências. Isto torna-se mais proeminente pelo uso mais vasto, o que quer dizer que estas perturbações têm tendência a agravarem-se no futuro. Um dos resultados é que perdas adicionais irão ocorrer e os utilizadores serão penalizados por isso porque terão de pagar mais. Há necessidade de reverter esta tendência também num esforço para ajudar a baixar a poluição. Outra consequência das perturbações é a dificuldade acrescida para o operador da rede elétrica em a manter estável. Portanto todos serão beneficiados por um consumo elétrico mais eficiente. Uma perturbação da qualidade de energia pode ser medida com um analisador de qualidade de energia o que ajuda o técnico a encontrar a sua causa. Este é o primeiro passo para encontrar uma solução para resolver a perturbação.

O objetivo deste projeto era implementar algoritmos de processamento digital de sinal numa FPGA para análise de perturbações da qualidade de energia. O motivo que levou à escolha da FPGA é que no mesmo circuito integrado é possível integrar um processador para as tarefas de processamento menos exigentes, e hardware dedicado para as operações criticas no tempo. A implementação destes algoritmos em hardware dedicado permite obter medições de alta resolução e explorar o paralelismo para aumentar a quantidade de informação disponível para o utilizador. A FPGA é um componente versátil, ideal para implementar o analisador da qualidade de energia reconfigurável que é atualizável no futuro.

O projeto resultou na medição com sucesso da frequência fundamental e a amplitude do sinal na entrada. O aparelho foi capaz de detetar e medir componentes harmónicos e inter-harmónicos. Valores de pico positivos e negativos foram medidos e o valor médio da raiz quadrada tanto para o ciclo completo como para meio ciclo foram calculados possibilitando a avaliação de variações estacionárias do sinal. Agregação temporal dos valores também foi efetuado. A geração de um sinal interno possibilitou a comparação com o sinal de entrada, que resultou no isolamento de eventos para posterior verificação e classificação pelo controlador.

Palavras-chave: energia, FPGA, monitor, perturbações, qualidade, variações

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List of acronyms

AC	Alternating Current
ADC	Analogue-to-Digital Converter
DC	Direct Current
DDS	Direct Digital Synthesizer
FFT	Fast Fourier Transform
FIR	Finite Input Response
FPGA	Field Programmable Gate Array
IEEE	Institute of Electrical and Electronics Engineers
LSB	Least Significant Bit
MSB	Most Significant Bit
PLL	Phase-locked Loop
rms	Root Mean Square
SOGI	Second-Order Generalized Integrator
THD	Total Harmonic Distortion
UART	Universal Asynchronous Receiver Transmitter
VCO	Voltage Controlled Oscillator

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1. Introduction

This chapter discusses the motivation for this project and presents the main objectives. The software tools that were used for the development of this work are also indicated. The chapter ends with a summary of the main topics discussed in each chapter contained in this document.

1.1. Motivation

Inevitably we are all dependant on a commodity that is so basic to us, after water, electricity! This form of energy is most likely the one that is easiest to convert into any other form of energy such as light, heat, mechanical energy or portable power. We all know what it would be like to be without it, or do we?

Electricity is an energy vector rather than an energy source. It has to be converted from a different form of energy like the burning of fossil fuels or produced from mechanical water flow or even from a nuclear reaction. In recent years renewable power sources are also more extensively used such as wind power, solar power or wave power.

Electricity has to be transported from the location of production to the main areas of consumption like the large urban areas of the world relying on a transport network. In the traditional system the electric power is produced in a small number of locations, generally at large distances from the main locations of consumption. These production plants are all connected to the transmission network across a country or a continent, which allows their resource to be shared over larger areas. This transmission system permits the price reduction of the electricity but is also an important contributor to the reliability of the power system [10].

At the locations of large consumption electricity needs to be distributed to reach every consumer's home and every industry. The distribution network is thus used to distribute electricity from the substations to the user loads. The distribution networks are usually radial in structure to distribute the energy over as large an area as possible. This allows the network to be easily operated and protected. The disadvantage is that in the event of any component failure several users can have their supply interrupted. Any problem within this process of transportation or distribution can cause major havoc.

With renewable energy production becoming more widely used, the distribution network has a slightly different function. It is now a network used for the exchange of energy between consumers and producers where consumers can be producers as well. It is possible for such consumers to consume the energy they produce and sell their excess over the network. Solar power for instance will only be able to be produced during daylight hours. Wind power on the other hand is generally more prominent at night or at sunset. The latter is a very intermittent form of energy production as wind might not be available for several days. These systems are sensitive and prone to disturbances which result in loss of

production when their network protection equipment acts. This creates a network stability issue in that their switching on and off simultaneously with variations can cause the network to destabilise and go offline. These systems also increase disturbances such as flicker, voltage variation and waveform distortion.

It is becoming more and more challenging to manage the electric grid effectively. The main function of the network is to maintain the voltage within acceptable limits and allow the current exchange between customers, where customers are producers and consumers. A variety of disturbances are also associated with the system.

Various reasons have led the quality of power to become a problem. Equipment is more intolerant to disturbances as they provoke failure in the sensitive electronic circuitry. Production processes are more intolerant to disturbances as productions are adversely affected by them. Businesses are more intolerant to the loss of production runs and production stops. The causes of the high costs associated to these problems are short and long term interruptions, voltage dips or transients. Modern equipment provokes higher distortion and noise in current because their power supplies, having become lighter and reduced in size, are electronic converters that work at high frequencies. These are the origin for high frequency interference resulting in harmonic distortion [16].

In later years there is a general tendency to use energy efficient equipment such as energy saving lamps or adjustable speed drives as well. Both produce disturbances in the supply and are sensitive to quality disturbances. When these issues cause a conflict in the broad introduction of environmentally friendly efficient technology, power quality becomes an environmental problem.

The truth is that consumers are more demanding than ever in that they request a good source of power with quality and at very affordable prices. Consumers also use more electricity than ever with tendency to increase in years to come. At the same time we have a duty to look after our planet by cutting down pollution completely. This makes it important for us all to use this energy source wisely and as efficiently as possible.

Deregulation has brought about the need for entities to create rules to orientate the duties of producers, suppliers and consumers of the network. Consumers are therefore more informed and more knowledgeable about what their rights are. This makes them more demanding [8].

There is a greater need for equipment that can analyse these various power quality parameters and distinguish between the different disturbances. There is an obvious tendency for these to increase in future. It is necessary to analyse power quality in detail at a specific location so that the sources of disturbances can be identified and corrective measures can then be taken to resolve the issues. Next, the discussion is on the definition of power quality and how power quality disturbances are separated into two groups.

1.1.1. Definition of Power Quality

Power quality has no one true definition. There are various versions, some of them conflicting with one another. The Institute of Electrical and Electronics Engineers indicates what to expect from the power supply, very broadly. If disturbances do not affect the operation of equipment they are not power quality issues. The International Electrotechnical Commission designates a set of parameters against which a system can have these parameters measured and quantified.

Power quality can be defined as being a combination of voltage quality and current quality. The ideal voltage waveform should be a sinusoidal wave of constant magnitude and constant frequency, where magnitude and frequency are equal to their nominal values. The ideal current is not also just of constant magnitude and constant frequency, but its frequency and phase should be the same as that of voltage. Any deviation thereof is a power quality disturbance [10].

A disturbance can be related to voltage or to current. As soon as current is affected it will reflect itself on the voltage. When a disturbance affects the voltage waveform it will reflect itself on the current. A voltage disturbance would be a sign that its origin was in the supply network while a current disturbance would indicate that its origin was from the load. This analogy has its flaws. A large load from a consumer starting up can cause current distortion which in turn will affect the voltage waveform. This will be seen by other consumers that the disturbance originated in the supply network. A disturbance can lead to consumers to be affected in different ways. It is important that the definition of power quality covers all disturbances present in a power network.

In Portugal, there is a specific regulation for the quality of service, fundamentally, by the Regulation of Quality of Service, a publication from the entity that regulates energy services (ERSE). It specifies automatic compensations to each consumer if the frequency and / or the duration of the interruptions are higher than a standard, defined by area. The information is audited by the regulator [8].

1.1.2. Power Quality Disturbances

Power quality disturbances can be divided into steady-state or almost steady-state variations that require a constant continuous measurement and sudden disturbances or events that have a beginning and an end. There seems to be consensus in this separation.

A typical example of a variation is a drift of the system frequency. Its nominal expected value is 50Hz. But this value has variations over time as load variates and generators accelerate or slow down within the system to adjust. The measurement of system frequency can be done at any moment and a value will be found. This value can be found periodically at every 10s with an even smaller sampling time [4]. Over a longer period like one day, various values will be available making it possible to calculate

statistical values for the frequency such as average or deviation. When measuring power quality it is necessary to extract the desired variation characteristics from the sampled signal. Here, frequency would have to be extracted from the sampled voltage. It is also necessary to create statistics that can calculate the performance of the supply and the system [10].

A typical example of an event is an interruption where the magnitude falls to zero. To be able to measure such an occurrence the measuring device has to wait for it to occur. Most power quality monitors have this type of function. A threshold is set; if the magnitude falls below that threshold an interruption is registered. Its duration is ended when the expected nominal magnitude returns to normal, above a second threshold. After long periods of measurement at various locations, statistics referred to the type of interruptions can be obtained. Interruptions with duration longer than a certain period might be the only ones of interest such as those over 3 minutes.

The separation between variations and events is sometimes not easy to make. A dip could be considered to be an extreme case of magnitude variation. To capture events some form of triggering is needed while for variations this is not necessary. This can help to distinguish between variations and events.

Power quality monitoring is done for several reasons: 1) to detect the reasons behind equipment malfunction; 2) to assess the network performance; 3) to verify settings of network protection equipment; and 4) to predict equipment failure.

Both end consumers and network operators may need to detect the reasons behind equipment malfunction, so that they can take adequate measures to deal with that issue. Network performance assessment is also an important task in order to analyse the stability of the network so that network operators can decide on measures to improve performance and lower customer compensation costs. The verification of network protection equipment settings is necessary to assure that they only act when it is entirely necessary to protect the network. Predicting equipment failure allows the network operator to plan and repair the problem before it can cause any problem to customers. Permanent monitoring allows for post analysis of the problem, understanding of the cause-effect through the system and explaining why it occurred [16].

1.2. Goals

The goals set out for this work were to use various modules to do digital signal processing (DSP) tasks on the signal expected at the input of the power quality monitor. The various results from these digital signal processing tasks would enable the identification of the various parameters associated with power quality. The modules to be used would be implemented on programmable logic devices, in this case Field Programmable Gate Arrays (FPGA).

An FPGA is a digital integrated circuit device that is based around a matrix of configurable logic blocks that are connected through programmable interconnections. FPGAs are reprogrammable which means that their functionality can be modified even after the device in which they are incorporated is manufactured. This makes them an ideal candidate to be used where future upgrades of equipment could be necessary. They also allow for a reduction of component use in the device, as they allow the designer to integrate custom digital functions and software functions within the device [18].

In this project, the FPGA is expected to integrate a soft-core microprocessor to deal with all non-time-critical tasks and custom hardware modules to deal with signal processing tasks, as shown in Figure 1. This figure illustrates the architecture of the whole system, as it is envisioned, although the aim of this thesis was to develop the digital signal processing modules alone. Also, the figure depicts a generic three-phase system, although this project has been developed considering single-phase systems only.

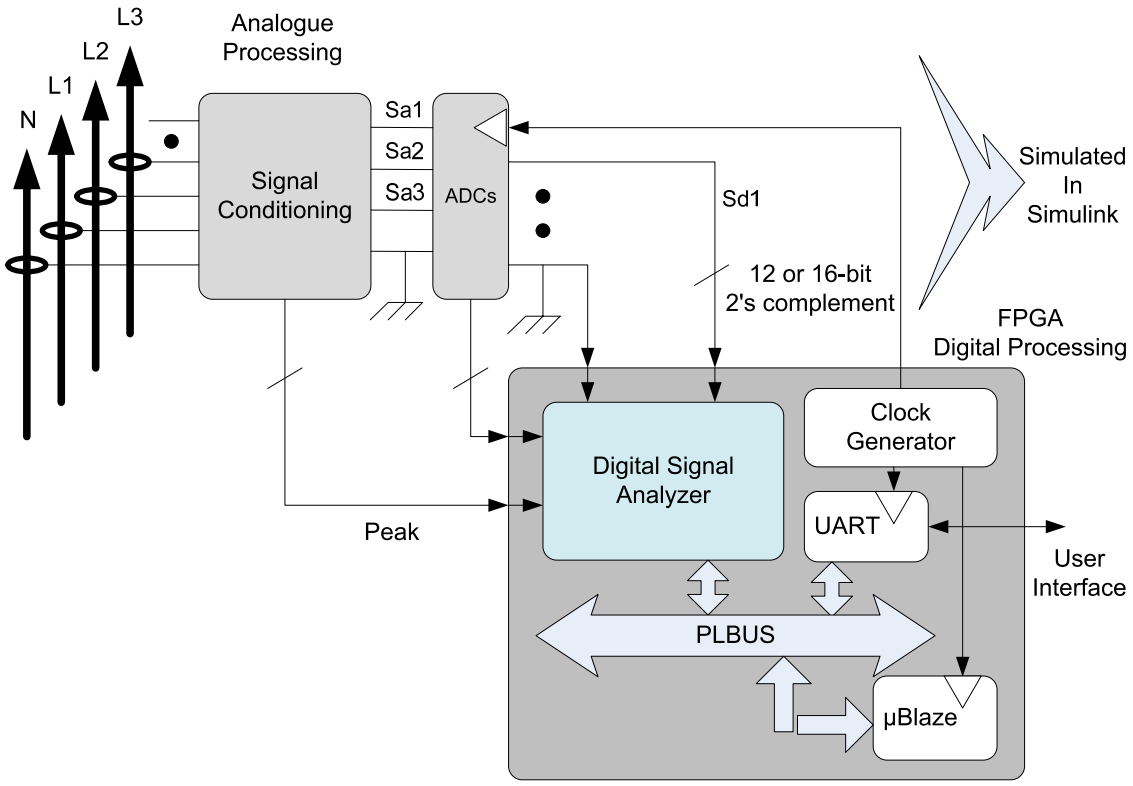

Figure 1 - The overall system architecture.

A typical three-phase power electric grid supply should consist of four insulated conductors or cables. Three of these cables are responsible for the supply of voltage and current of each of the three phases supplied to the consumer, while the fourth cable is responsible for neutral which is the feedback circuit. This later path can be supplied by the network or in some cases can be created locally depending on the connections used. This is invariably so for most industrial consumers as many of the motors, welding machines or variable speed drives used in industry are three-phase devices. A fifth cable may also be

used for the earth connection. Generally this voltage level is obtained locally where the electric grid delivers the supply to the consumer.

Voltage can be measured through a parallel connection at any point where the physical conductor itself is visible. The measurement for current is done with a series connection but this would make power quality monitoring a literally impossible task. It would not be very sensible to stop supply to the consumer just to connect the measuring device and then again when the measuring system is removed. A system through induction, similar to the functioning of a transformer, can be used as a non-obtrusive method of obtaining the current values. Current clamps are readily available from most test equipment manufacturers. They are not all the same; some have a larger ring clamp to embrace larger diameter conductors while others have smaller diameters. They are also available with different scaling ratios like 1000:1 or 10.000:1. This is needed to be able to measure very large values without destroying the test equipment. The test equipment in many cases is unable to measure values higher than a few hundred volts at its inputs. Careful handling is always necessary to make these connections and user safety has to be of utmost priority. Incorrect handling can cause death.

After the attenuation of these signals either by the current clamps or the measuring device itself should be analogically processed and conditioned. Detection of high peak values should be done here and if necessary removed. Control signals indicating that excessive peaks, beyond the dynamic range, were measured indicating the peak, the value, the time duration and the instant. Transimpedance amplifiers with gain or attenuation should also be used to convert the current value into an equivalent voltage signal.

A low-pass filter should be used to remove all high frequencies that are not to be measured. The highest harmonic, inter-harmonic and mains signalling frequencies must be known so that they can be allowed through to be measured. All other frequencies above this value must be removed. If not, a duplicate component of these frequencies can appear lower down the spectrum when the sampling frequency is not above two times the highest frequency (a phenomenon usually known as aliasing). These ghost components will cause great difficulty to obtain correct measurements as they simply do not belong there [13].

After the conditioning of the analogue signals have been done, the results are analogue signals that represent the values of the electric grid supply. These signals have peak values limited to a dynamic range that the Analogue-to-Digital Converter (ADC) is able to use. Normally this range would be 0 to 3.3V for portable devices. This means that all analogue values at the input of the ADC will be within 0V and 3.3V, never beyond. The dynamic range of the ADC should be 1.2 times larger than the nominal signal to be measured so that a tolerance of 20% higher values can be measured. If this tolerance is larger, very high peak values can be measured but resolution is lost for the values from zero to the nominal. If there were no tolerance, maximum resolution of the signal between zero and nominal values could be achieved but no peak values would be measured. It is always a trade-off but 20% seems to be reasonable.

The output of the ADC results in digitally sampled signals that represent the values at its inputs. These samples are 12 or 16 bit wide digital values in two's complement. The more bits compose the sample the better the resolution of the signal will be as more intermediate values will be available between maximum and minimum. For this work a 16 bit ADC was presumed to be used as these are readily available at affordable prices.

The digitized samples of the measured values are presented to the FPGA. The digital signal analyzer is composed of digital signal processing modules that will process the signals, extract the relevant data and make this data available for the processor to use. These digital signal processing modules are peripheral units to the processor. Because the digital signal processing is done in hardware, the measurement resolution is limited only by the FPGA clock frequency and the degree of parallelism that can be used in implemented algorithms.

The Spartan 6 FPGA was the device chosen from the Xilinx range for this project. The FPGA is a versatile programmable device that can be reprogrammed, becoming an excellent device to use in future upgrades if they are considered to be necessary. It is a device that can be configured to have various electronic peripherals and processors. The FPGA has a two-dimensional array of configurable resources to implement complex arithmetic routines and logic functions. Resources include DSP blocks, lookup tables, multipliers, registers and dual port memories to name a few. The FPGA has a sophisticated input and output bus that can handle a wide range of bandwidth. It also includes embedded microcontrollers and has a programmable interconnect structure with system frequencies running as high as 100 to 200MHz.

The digital signal processing operation is a continuous process that continues to identify power quality parameters by extracting the relevant data and values. This information is then available for the processor to use according to the end-user's request. Aggregation of data into statistic values over a period of time is also done by the hardware peripheral modules so that the processor does not have to do this work.

The processor then interacts with the user and the outside world through the Universal Asynchronous Receiver Transmitter (UART) to supply the data in any form found convenient. The UART allows for serial two-way communication with the respective handshakes necessary for the communication to run smoothly. The data fed from the processor can be sent to an external Personal Computer (PC) or a display. The processor will also have the responsibility to do complex calculations when these are necessary and considered to be more efficiently done in software, rather than in hardware.

A general clock generator would be used to generate the correct clock signal to synchronize all internal modules, the processor and external devices with the respective clock.

1.3. Software Tools

Various software tools were necessary for the development of this project. Xilinx and Mathworks development software was used to technically implement the first part of this work. The packages were System Generator from Xilinx, Matlab and Simulink from Mathworks. Their versions were Matlab R2013a with embedded Simulink version 8.1. The System Generator used was part of Xilinx ISE 14.6. The second group of software was used for the writing of this document. Microsoft Word 2007 was used for the actual writing and formatting. Spell checking was also done with the aid of this software. The gathering of data and its analysis was done with Microsoft Excel 2007. Finally a drawing package, Microsoft Visio 2007, was used for the drawing of diagrams and figures. They were chosen to be of the same group so that compatibility between them would not be an issue.

Matlab, developed by Mathworks, is a multi-concept numerical computing environment and high level programming language. Matlab stands for Matrix Laboratory and is a widely used technical tool in industry and education. This instrument is used by scientists, economists and engineers of various fields. It is an excellent tool for matrix manipulation. It is used for complex algorithm development and implementation. Plotting of functions or data can also be accomplished with it. It is able to interface with other programming languages used in technical programming such as C, C++ or Python and can be used for creating user interfaces.

Simulink is an integrated package in Matlab that is a graphical multi-field simulation tool. It is a graphical programming language that can be used to develop models. Simulation of the models and dynamic systems then allows for the analysis of the resulting data. It has an extensive block library with toolboxes of various engineering and scientific fields. Programming is done by selecting the required blocks into a worksheet, connecting the blocks adequately and simulating the model. Complex dynamic systems can be simulated this way without writing one line of code. It can be used in the fields of automation, digital signal processing, mechanical systems, image processing and embedded processing to name only a few.

System Generator is a tool from Xilinx ISE. It is a high-level tool used for the design of high performance Xilinx DSP programmable device systems by using Simulink as the foundation. It is used to develop DSP algorithms that can be modelled and tested through the use of graphical blocks. Emulation of models can be done to test the system before it is implemented. Code can be automatically generated after the design has been finalized without having to write any code [19].

The word processor used was Microsoft Word 2007 and it forms part of Microsoft Office. It is a widely used package, designed for the writing of documents. Predefined templates and formatting tools are available to assist the user. A selection of various fonts and sizes are also available. Images or objects can also be included. An assistant to introduce formula and symbols is also integrated in this package. Page layouts can be

defined as well as margin sizes or printing preferences. It is a good overall package for writing reports.

Microsoft Excel 2007 is the spreadsheet that also belongs to Microsoft Office. It is an excellent tool for data manipulation and calculation. It is good for displaying data in graphs. It consists of a matrix of cells into which data can be introduced. The numerical values can then be manipulated arithmetically with other values in other cells. Matrixes can be manipulated, macros can be written to do certain routines. The program can also find a best solution to a complex problem where different variants need to be taken into account. It is a widely used tool in the economic, engineering and scientific fields also. Various sheets can be used in one file turning it into a book of spreadsheets.

Microsoft Visio 2007 is a software package designed for drawing diagrams. Its main function is for the creation of technical vector graphic images. The package has a wide selection of templates and shapes for flow diagrams, organization hierarchical structures, electric and electronic components for signal diagrams and architectural layout for buildings or even IT networks. It is a simple and flexible tool to use for rapid quality diagram design used for the drawing of the figures.

1.4. Thesis Organization

The thesis is organized into five logical chapters, each of which deals with a specific part of the project.

The introductory chapter deals with the motivation behind this project. It contextualized the problems that are associated with power quality in the grid supply network. It also mentioned the overall objectives and goals for measuring power quality disturbances by using a programmable logic FPGA device. The overall proposed structure for the system was also explained. The various software packages used during the project were also identified.

The second chapter deals with the power quality concepts. Power quality disturbances are divided into two main groups of phenomena: 1) gradual deviation variations such as magnitude, frequency and harmonics; 2) the abrupt once-of events such as dips, swells, interruptions, flicker and transients. The origin and the effects of the disturbances are also discussed. The international European Standards were identified, analysed and discussed. Two of the commercially available instruments were also evaluated.

Chapter three focuses on the implementation of the signal processing units. It begins explaining the implementation details of the stationary signal measurement and parameter capture units. Their characteristics and their limitations are also identified and discussed. The reasons for data aggregation are indicated and their implementation shown. Finally the implementation of the modules for the processing of events that permit the detection and measurement of events are explained.

The fourth chapter looks at the test results. The test signals used for simulation purposes from Simulink are enumerated and explained. These signals are used during the emulation of the FPGA function blocks. The measurements for site indices are shown and commented such as frequency, magnitude peak values and rms. These power quality parameters were verified under various situations. Their limits are explained and the reasons for their existence also. The characteristics and limitations of the FFT in measuring harmonics and inter-harmonics are shown with the respective results. The characteristics and limitations of the PLL in event detection are also shown with the respective results.

The fifth and last chapter ends with the conclusions and a final discussion on how the processor could use the results of the hardware peripherals to identify the power quality events and how the user could have access to the information. The main conclusions for this project are made as well and future work identified.

2. Power Quality

Power quality is concerned with the supply of electricity in its ideal form to every customer. The modern customer's expectation is to receive an alternating voltage of acceptable magnitude and at a determined frequency so that he has energy to switch on any electrical device he chooses and when he chooses. The expectation is that the current waveform associated with this voltage bears some resemblance with it. This chapter will describe the fundamental concepts of stationary and non-stationary voltage variations. It also discusses the European and international standards and ends with a comparison between two commercially available monitoring systems.

2.1. Fundamental Concepts

When the supply deviates from the ideal, it can be for a number of reasons such as failure of power network components, earth faults, lightning and natural disasters, faults caused by customers or switching (on or off) of very large loads. These phenomena have been identified and are used during the monitoring process of the power quality. The voltage is measured to verify if there are variations in its frequency or if there are variations in the magnitude. Examples are dips, swells or even distortion of the waveform. The signals obtained through measurement can be separated into two main groups, the stationary and the non-stationary phenomena. Although the slow variations are not truly steady-state disturbances or stationary phenomena, they can be considered as such, because the frequencies involved are lower than 50Hz. The fast variations can then be considered to be sudden disturbances or events that have a beginning and an end.

Stationary phenomena include those phenomena associated with gradual variations over a relatively long period of time such as the variation in frequency or small variations of the nominal magnitude. These values are expected to be very close to predetermined values or to be within acceptable tolerances. Harmonic and inter-harmonic content can also be included within stationary phenomena [10].

Non-stationary phenomena include those phenomena associated with variations that are abrupt, occurring in short periods of time. Such deviations include those measured during dips and swells, transients and overvoltage, flicker, interruptions and distortion, among others [10].

This section will discuss stationary phenomenon variations in more detail, their causes and identify examples. Thereafter non-stationary phenomenon variations will also be discussed.

2.1.1. Stationary Phenomena

A stationary phenomenon, although measured in a short window of time is considered to continue before and after the window. This would allow it to be processed with the same method in each consecutive window. In reality stationary phenomena in the power system do not exist as they are affected by slight variations over time. Stationary phenomenon perception is associated to the tolerance levels in frequency and wave magnitude measurements. The changes that occur between consecutive windows of measurement are almost negligible. The parameters associated to the quality of stationary phenomena are shown in Figure 2. They are: a) frequency; b) voltage magnitude; c) harmonics; d) inter-harmonics; e) flicker.

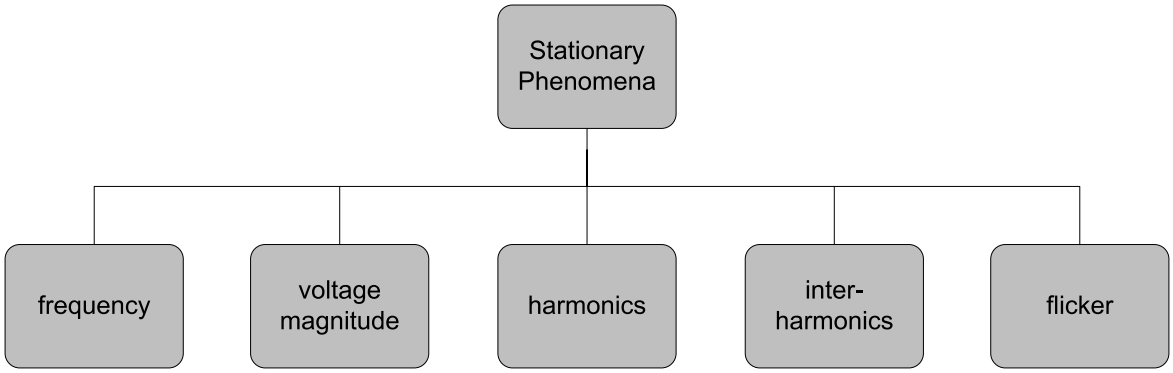

Figure 2 - Parameters associated to stationary phenomena.

To start, in the electric grid network the electricity produced has to be consumed as this energy cannot easily be kept in large amounts for later use. The production of this energy is based mainly on rotating mechanical machinery; from generators to water or steam turbines. They convert mechanical energy into electrical energy to maintain the balance between production and consumption. When synchronous machines are used, the speed at which these devices rotate is directly proportional to the frequency of the alternating voltage they produce. The rotation of these machines is generally very well controlled which means that significant frequency variations are not very common. A very large load disconnecting from the grid can cause a sudden increase in frequency due to less energy being consumed from the grid. When this happens, actuators on the primary machine ensure that the rotation of the machines in the system is decelerated to compensate for the lower amount of energy that has to be produced. When a very large load is switched on in the grid there is a decrease in frequency due to the increase in consumed energy. When this happens, the rotation of the machines in the system has to be accelerated to maintain the frequency at the nominal value. All electricity equipment, producing or consuming, is intrinsically kept synchronized. Each full turn of a machine in the system produces an integer even number of equivalent sinusoidal wave periods in the system. Frequency is therefore the repetition of these sinusoidal wave periods per second that is dependent on the speed of the generators within the system. In the majority of the European countries frequency is expected to be kept at 50Hz [12].

Variations in frequency can cause clocks that synchronize to the system frequency to slow down or to speed up; it all depends on how far the frequency deviates from the nominal value. This happens in clocks that are synchronized with the zero-crossings of the sinusoidal wave. Alternating Current (AC) electric motors will also be influenced by variations in frequency by speeding up or slowing down as the frequency changes. This could be a problem in production lines that include rigorously timed processes controlled by the speed of the motors. Such an example could be the automotive industry where various processes have to be carried out from the sheet metal work to welding and painting [16]. Magnetic flux in motors and transformers can also increase due to a lowering frequency. This would cause an increase in magnetization currents. Large deviations can cause generators or loads to trip depending on their settings. Normally loads have relays that are set to trip at low frequency limits, to save the network when it is not able to recover fast enough, due to sudden increases in consumption or loss of a large generator. The rate of change of the frequency, if fast, could affect the performance of some equipment using Phase-Locked Loop (PLL) circuits. A sudden change in frequency would be interpreted by that equipment as a phase shift. Small frequency deviations can therefore cause small problems but large deviations can cause instability within the electric grid and ultimately total shut-down [10].

The magnitude of the voltage is taken as the distance between sinusoidal wave crests above and below the zero reference line as a value that is calculated as a root mean square (rms) value, in other words the equivalent rectified direct current (DC) value. Overvoltage increases the risk of insulation failure on cables, transformers and motors over a long period of time. It also increases the base from which a transient can occur by increasing the peak voltage which can cause insulation failure. Overvoltage in induction motors can lead them to have increased torque on start-up that will increase start-up currents which can consequently drop voltage in loads in the vicinity of the motor. Undervoltage on the other hand, can lead them to have poor acceleration or to heating up. The light output of lamps and the lamp life are affected by voltage variations, some slightly more than others. Heat generated by resistance heaters can be affected by undervoltage. Heat decays in a larger proportion than voltage with an approximate ratio of 2:1. Equipment with thermostats will most likely work for longer times with undervoltage, increasing their energy consumption. Electronic equipment too can reduce performance when affected by undervoltage while overvoltage can reduce their life expectancy. A high nominal voltage on transformers causes increased magnetizing currents that distort the waveform. Voltage fluctuations can cause light flicker, caused by the repetitive action of equipment switching on and off. This is possible from equipment such as refrigerators and air-conditioners where the motors work intermittently to control temperature between two relatively close threshold temperatures. The result would be a flicker effect on lights in the immediate vicinity. Other problems can also arise, such as control circuits that use the voltage angle or the time for acceleration / braking of a motor. Small deviations in voltage magnitude cause minor problems but large deviations can cause equipment damage or to shut down [6].

Waveform distortion can take place in voltage and in current. Voltage waveform distortion means the electric grid affects the customer or his load while current waveform distortion implies that the customer affects the electric grid. Waveform distortion includes harmonic, inter-harmonic and non-periodic distortion. The non-periodic distortion will be considered under events. A non-sinusoidal wave that is periodic can be decomposed into the sum of its harmonic components. The majority of waves contain a fundamental frequency sine wave that is otherwise known as harmonic 1. This is usually the dominating component in the case of the voltage. Harmonic components are multiple integers of the fundamental wave, while inter-harmonic components are not. Harmonic components can be divided into two groups, even and odd harmonics. Generally the odd harmonics will be more prominent. Odd harmonics affect the positive and negative half-cycles of the wave in the same way but even harmonics affect the half-waves differently. The waveform is composed of its fundamental component, harmonic and inter-harmonic components.

Transformers react to harmonics by becoming noisier and by warming up more. Overheating of the transformers is caused by stray magnetic flux caused by higher frequency harmonic components. Because the heating is not necessarily uniform, transformers have to be underrated to cope with this effect. Similar heating effects are caused on cables and lines. The harmonics provoke a skin effect causing currents to flow mainly on the outer perimeter of the conductors. Neutral conductors in three-phase systems will accumulate the triples of harmonic currents from the three individual phases. This particularly occurs when many computers or energy-saving lamps are in use. This can lead to overheating of the neutral conductor with overload protection aimed at protecting phase conductors only, not tripping. Neutral currents caused by the third harmonic can cause magnetic fields and neutral to ground voltages. The magnetic fields can affect sensitive electronic equipment such as computer screens.

Electronic equipment using zero-crossing information could be affected by distortion if the zero crossing point should shift or if there are multiple zero crossings. High frequency voltages can couple to electronic or logic circuits causing them to fail. High harmonic content can cause a whole variety of electronic equipment to fail such as medical equipment with its obvious consequences. Computers, television and other audio and video equipment can be also affected. High frequency ripple from rectifiers can cause electronic circuit tripping of gas burners. Very high distortion can cause certain compact fluorescent lamps to stop working. Most modern equipment consumes current when the voltage magnitude is high which in turn causes a flattening result in the voltage waveform. Since internal dc is directly proportional to the AC maximum, the reduced DC affects the device to operate less efficiently and become more prone to voltage dips. The loading on the power supply increases, reducing its life expectancy. Peak voltage variations can cause picture size and brightness variations on television or computer screens.

Signalling and communication over the power lines could be affected by waveform distortion. High distortion could be confused with control signals in the electric grid. Interference in telephones can occur if the distortion frequencies fall into the audio range. This is particularly evident if single phase overhead lines share the same poles as telephone

lines. High frequency harmonics can destroy capacitors by causing a heating effect on them. The harmonics also destroy the dielectric in capacitors. Capacitors can amplify these harmonic components by series and parallel resonance. The main effects caused by waveform distortion on rotating machines are oscillations in the torque and noise which could damage them. In single-phase induction motors this is more evident due to capacitors being present that resonate with leakage inductances from the motor, resulting in larger losses. Harmonic and inter-harmonic components can cause equipment damage [10].

2.1.2. Non-stationary Phenomena

In this context, non-stationary phenomena as opposed to stationary phenomena are those that contain great non-repeatable deviations to the expected wave. Generally these deviations are fast disturbances or events that can occur once only or are repetitive during very short periods of time. Examples of such disturbances are voltage dips, swells, interruptions and transients. Non-stationary phenomena, or events by which they can also be identified, are non-repetitive exceptions to the expected waveform shape. Parameters associated to non-stationary phenomena are indicated in Figure 3. They are: a) dips; b) swells; c) transients; d) interruptions.

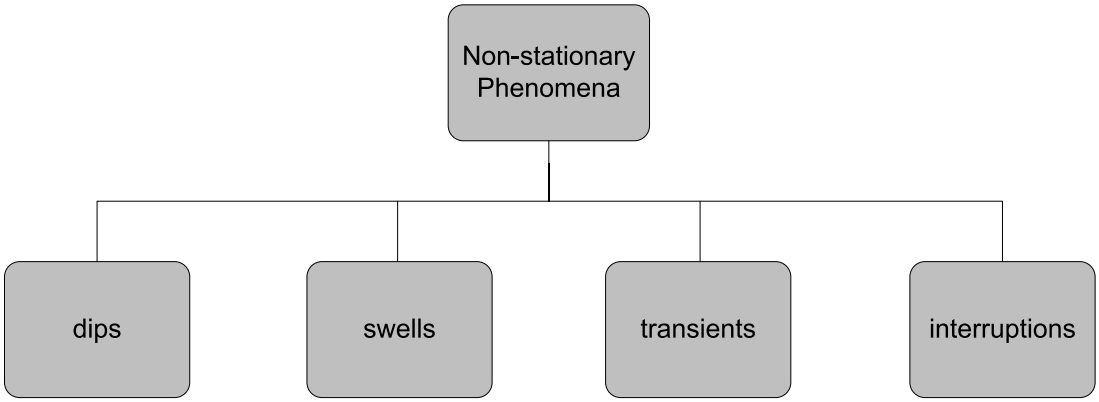

Figure 3 - Parameters associated to non-stationary phenomena.

An interruption is considered to be a voltage magnitude drop to below 5% [3] or very close to zero. In reliability studies from the network point of view, this more generally means that there is a galvanic disconnection from the customer. For customers, the two are the same as a disconnection also rapidly resembles zero voltage. For customers with their own generation, the situation can be different. The generator and the local system load are disconnected from the network. A new steady-state in the system has to therefore be reached to obtain acceptable voltage magnitude and frequency. Interruptions can be divided into two types, short and long term interruptions. Interruptions cause electric and electronic equipment to stop working [10].

A short circuit or earth fault can cause a circuit breaker or a fuse to open causing a disconnection between a customer or a group of customers and the network. Incorrect manual operation or an incorrect tripping signal due to a fault can also cause a circuit breaker to open. For repair purposes part of the system may be intentionally disconnected.

This latter one can be considered to be a planned interruption where the others would be considered to be forced interruptions. The length of the interruption depends on whether the system is restored automatically or if it has to be restored manually. The time needed for the last one will be longer, of course. An interruption can be caused by numerous incidents.

Voltage dips refer to a lowering of the voltage magnitude during a short period of time typically no longer than 1s. The remaining voltage magnitude can vary from anywhere close to the nominal value to close to zero. Voltage dips cause production stoppages in industrial clients and may cause damage to electronic equipment. Typically the monitoring threshold for a dip is 90% of the nominal value. A voltage dip is caused by an increase in current consumption normally elsewhere in the system for a short period of time. The increase in current by one user will affect the other users on the same distribution bus in the network. A short circuit or an earth fault, the starting up of an induction motor or the energizing of transformers can be the cause of this current increase. Voltage dip duration can be from a few cycles to a few seconds. The majority of faults that cause dips are cleared by the power systems' protections or can simply disappear before any protection devices can act. Typically these faults are of very short duration and very unstable in nature. Voltage dips can destabilise equipment functions without causing it to shut down entirely [10].

Large single-phase loads in single-phase household systems can cause short duration voltage dips during starting and during their operation. Such devices may vary from the kettle to a refrigerator or a vacuum cleaner. Transformer energizing or the starting of a motor can cause a sudden voltage dip with a gradual recovery thereafter. Voltage dips can be caused within the customer's installation.

As opposed to voltage dips, swells can also be observed in the power grid. Single-phase faults consequently cause swells of short duration. Long duration swells can be observed when there are losses of large loads in the system. Swells can also cause equipment to malfunction or just become unstable.

A transient refers to a disturbance in the steady state of the voltage or current during a short time. Generally these take place during one half-cycle or last as long as one full cycle. A transient overvoltage is associated to an overvoltage with a peak that has a rapidly decreasing oscillatory nature. A similar effect is usually seen on the current waveform. Transient overvoltages can be classified as lightning transient overvoltages or switching transient overvoltages. As their name implies the lightning transient overvoltages are associated to the effect of the electric energy discharge from a lightning strike, either directly or indirectly, on the electric grid. Overhead lines are the most vulnerable during the lightning storms. Switching transients are caused by switchgear in the network that changes state while loads and generators are still connected. A transient overvoltage is also sometimes referred to as a surge. Transient overvoltages are sudden energy peaks superimposed on the expected waveform that rapidly disappear [11].

When lightning strikes an overhead line or in the vicinity thereof, the overvoltage frequently causes a short circuit fault or an earth fault on the electric grid. This usually leads to the action of protections that then cause a dip in the system. Normally the rise times of these types of transients are very fast, around 1 μs with a slower decay. Low impedance earths of shielded cables and antenna towers reduce the strength of the transients by supplying a current path to ground. The voltage transients caused by lightning strikes from indirect hits reach the lines by induction. Both direct and indirect lightning strikes can cause major damage to equipment when reaching equipment through the power lines or through an increase in earth potential. The most severe switching transients are undoubtedly those that are associated with capacitor charging. The transient oscillation can be a few hundred hertz. Transients are more prominent with more capacitors in the system due to the amplifying effect they have. Capacitor discharge transients are usually less severe and depend on the two steady-states voltages before and after switching. Transient are less severe when associated to inductor energy. Transients cause severe equipment damage.

Most of these exceptional characteristics in electric power systems are rather short in nature but can have a high occurrence rate. In power quality monitoring the data accumulated over one day or one week is immense. For this reason aggregation periods are needed for statistical evaluation of the system to conclude whether or not there is a need to analyse a particular occurrence in more detail [10].

The amount of data resulting from the measurements is immense. It is generally very difficult to keep so much data stored in a power quality monitor, although these problems are easing in recent years. Data reduction is therefore necessary. A first reduction can involve not storing all the data. A second step should involve time aggregation of data which is a process in which a characteristic is obtained over time such as a value averaged over 200ms, 1s, 3s, 10s, 1 min., 10 min. or 2h. The next step to reduce data even further would be to describe power quality over the whole period with a limited number of indices. Such site indices can include average, median, maximum and 95% of the value, all the time.

The time aggregation of data is the process of obtaining a representative characteristic over a period of time to replace basic characteristics. Although it is more general, averaging can be used as a form of aggregation that is normally only used for the step from the basic characteristics to the characteristics represented over time, the site indices. Although storage of data is less concerning, the amount of data still requires some reduction or statistical processing. Too much data makes it difficult for interpretation. Due to disturbance levels being rather constant over the time scales, some defend that the lower time aggregation periods are unnecessary.

Statistics from basic or aggregated characteristics over a measurement interval recorded at a site are site indices. Such periods are typically one day, one week or one year. The main aim of site indices is to acquire a representative value that can quantify the

power quality for a site regarding one or more disturbances and their derivation can fall into one of three methods:

- Site index obtained as an average or median value.
- Site index obtained as a maximum value.
- Site index obtained as a ratio of a high percentage.

Site indices can be used to follow trends or to compare sites [10].

2.2. International Standards

With an ever growing concern on power quality, standards have been drawn up by various entities. The intention is to try to regulate the energy market in the use of the structure in an attempt to protect both producer and consumer. In later years the tendency has been to deregulate the market in production and supply which makes it even more important to have rules established. Consumers are also less tolerant to problems in the electricity supply while demanding low prices.

Both Europe and the United States have the more widely used standards. In some aspects they have some differences from each other, while in most cases both are very similar. These standards get revised from time to time in an attempt to keep them updated with market needs. The range of parameter values will be discussed, followed by a discussion on the measurement methods.

2.2.1. Parameter Values

Although the intention was to define the limits for power quality characteristics, some of them are not clearly delimited while others still need to be limited more tightly. EN50160 is the norm used in Europe to define and specify the main characteristics of voltage on the electric grid expected from the consumer's point of view. This document can be used in litigation processes between producers and consumers.

The main standards to define power quality in Europe are indicated in Table 1. EN50160 deals with characteristic definition and specification. EN61000-4-30 deals with the measurement methods and techniques to verify power quality. EN61000-4-7 is a general guide on harmonic and inter-harmonic components while EN61000-4-15 deals with the testing and measurement techniques specific to flicker.

Table 1 - Main European power quality measuring standards.

Standard	Latest	Title
EN 50160	2010	Voltage characteristics of electricity supplied by public electricity networks.
IEC 61000-4-30	2008	Electromagnetic compatibility (EMC) – Part 4-30: Testing and measurement techniques - Power quality measurement methods.
IEC 61000-4-15	2010	Electromagnetic compatibility (EMC) – Part 4-15: Testing and measurement techniques - Flickermeter - functional and design specifications.
IEC 61000-4-7	2002	Electromagnetic compatibility (EMC) – Part 4-7: Testing and measurement techniques - General guide on harmonics and inter-harmonics measurements and instrumentation, for power supply systems and equipment connected thereto.

Various characteristics and parameters are identified in the European EN50160 Standard. Supply voltage is characterized by frequency and magnitude where frequency is defined as the number of sinusoidal cycles per second of the AC supply voltage. Magnitude is taken as the root mean square value of the wave. Power quality parameters describe phenomena that can occur in the power distribution network.

European Standard EN61000-4-30 defines the methods for measurement and interpretation of the results for power quality parameters in alternating current power systems. The power systems referred to work with frequencies of 50 Hz and 60 Hz. The measurement methods are limited to conducted phenomena and do not include phenomena by induction except lightning because of its adverse effects.

European Standard EN61000-4-15 defines a functional design specification for a flicker measuring device. The device is intended to indicate the correct perception level for all fluctuation waveforms. The specification only relates to measurements on 120 V and 230 V systems with frequencies of 50 Hz and 60 Hz. A correction factor is also introduced in this standard. The implementation of this design was kept outside the scope of this project.

European Standard EN61000-4-7 is applicable to instrumentation intended for measuring spectral components in the frequency range up to 9 kHz which are superimposed on the fundamental frequency. It distinguishes between harmonics up to order 50, inter-harmonics and other components above harmonic frequency range, all below 9 kHz.

In general measurement devices are separated into two classes. The two classes of measurement performance are defined for each parameter. Class A is the more precise of these two classes, used when precise measurements are needed and for verification of compliance to the standards. This is the class stipulated to resolve disputes between supplier and consumer. Two class A devices must be able to present exactly the same results for the same measurement. Class B measurement methods are mainly left to the

manufacturer's discretion. Devices in this class are generally only used for statistical purposes or troubleshooting [13].

Even the organization of the measurements is defined through the use of measurement transducers connected directly to the supply network to scale down the values. These also help to isolate the measuring instrument from direct contact with the supply. The monitor then measures these signals to produce a measurement result. The measurement result is then evaluated to supply its result. Figure 4 shows this layout.

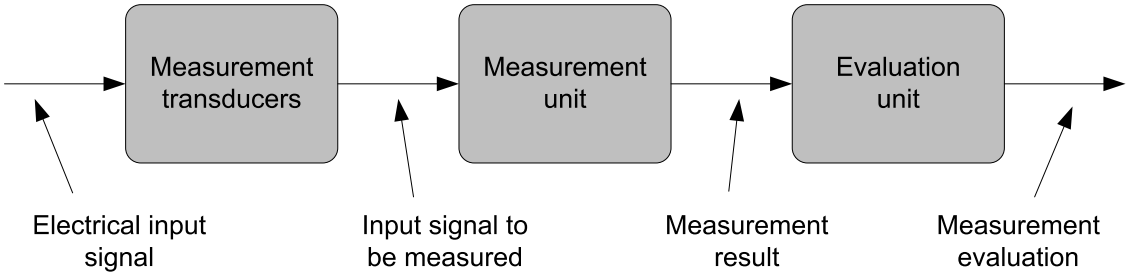

Figure 4 - Measurement layout chain.

Various parameters are identified such as dips and swells, interruptions, harmonic and inter-harmonic components, flicker, transients, rapid voltage changes and power line communication. Although the standard defines acceptable limits for these parameters, some have only indicative values and are not limited at all. Table 2 shows these parameters with their indicative values: a) rapid voltage changes, for the low voltage supply are defined as the single rapid variation in voltage magnitude for undefined periods of time; b) dips, the decreasing of the magnitude from anywhere between the rapid voltage change limit all the way down to just before the interruption limits; c) flicker, the short-term severity is defined as a visual sensation of unsteadiness noticed mainly in light from lamps over time. The flicker severity is defined as the intensity of the annoyance from flicker [14]; d) interruptions, defined as a condition where the supply voltage falls below 5%; e) swells, increase in magnitude from anywhere between the rapid voltage change limit all the way up to an additional 20% of the expected magnitude; f) overvoltage, on the low voltage supply is considered to be a fault where the neutral is momentarily replaced by a second phase and a transient overvoltage is defined as oscillatory or non-oscillatory overvoltage that is usually highly damped that can last up to a few milliseconds; and g) mains signalling, defined as the superimposed signal on the supply voltage to transmit data over the public network, generally only used by the network operators [13].

Table 2 - Parameters with indicative values.

CONTINUOUS PHENOMENA		
Rapid voltage change (Low voltage supply)		
230V ± 5%	i.e. 218.5V...241.5V	most of the time
230V ± 10%	i.e. 207V...253V	sometimes a day
EVENTS		
Dip		
$5\% \leq U_n < 90\%$	i.e. 11.5V...207V	(refer to Table 3)
Flicker, short-term severity		
P_{st}		measured over 10 min.
Short interruption		
$U_n < 5\%$	i.e. 0V...11.5V	< 3 min.
Long interruption		
$U_n < 5\%$	i.e. 0V...11.5V	> 3 min.
Swell		
$110\% \leq U_n < 120\%$	i.e. 253V...276V	(refer to Table 4)
Overvoltage (Low voltage supply)		
L-N ➤ L-L	i.e. 230V...440V, generally not exceeding $1.5kV_{rms}$	Typically no more than 5s
Transient overvoltage (Low voltage supply)		
L-N ➤ blow fuse, switching or lightning	i.e. generally not exceeding 6kV peak	rise time < 1μs (lightning) rise time > 1ms (switching)
Mains signalling		
ripple control	i.e. 110Hz...3kHz	99% of day, 3s mean
power-line carrier	i.e. 3kHz...148.5kHz i.e. 95kHz...148.5kHz, $1.4V_{rms}$	99% of day, 3s mean
mains marking	i.e. superimposed transients at selected points	99% of day, 3s mean

Although a classification table was created to organize the voltage dips, the standard foresees that this table would be used as a recommendation in the case of existing equipment. Table 3 shows the classification proposed by the standard. A combination between residual voltage percentages at the consumer for a duration period forms the matrix to count the number of dips registered during the measurement period [4].

Table 3 - EN50160 dip classification table.

Residual voltage u %	**Duration t** s				
	$0.01 \leq t \leq 0.2$	$0.2 \leq t \leq 0.5$	$0.5 \leq t \leq 1$	$1 \leq t \leq 5$	$5 \leq t \leq 60$
$90 > u \geq 80$	A1	A2	A3	A4	A5
$80 > u \geq 70$	B1	B2	B3	B4	B5
$70 > u \geq 40$	C1	C2	C3	C4	C5
$40 > u \geq 5$	D1	D2	D3	D4	D5
$5 > u$	X1	X2	X3	X4	X5

A classification table is also presented to organize the voltage swells. Table 4 shows the classification proposed by the standard. The combination between increased magnitude percentages at the consumer for a duration period forms the matrix to count the number of swells detected during the measurement period [4].

Table 4 - EN50160 swell classification table.

Swell voltage u %	**Duration t** s		
	$0.01 \leq t\ 0.5$	$0.5 < t \leq 5$	$5 < t \leq 60$
$u \geq 120$	S1	S2	S3
$120 > u > 110$	T1	T2	T3

The parameters that have defined limits are presented in Table 5. They are: a) the frequency, for systems with and without a synchronous connection; b) voltage magnitude; c) harmonic voltages; d) flicker, long-term severity as defined for short-term flicker but over a longer period; e) voltage unbalance.

Table 5 - Parameters with limits.

CONTINUOUS PHENOMENA		
Frequency (Systems with synchronous connection)		
50Hz ± 1%	i.e. 49.5Hz...50.5Hz	during 99.5% of a year
50Hz + 4% / - 6%	i.e. 47Hz...52Hz	during 100% of the time
Frequency (Systems with no synchronous connection, as on certain islands)		
50Hz ± 2%	i.e. 49Hz...51 Hz	during 95% of a week
50Hz ± 15%	i.e. 42.5Hz...57.5Hz	during 100% of the time
Magnitude		
230V ± 10%	i.e. 207V...253V	95% of 10 min. mean rms
230V + 10% / - 15%	i.e. 195.5V...253V	100% of 10 min. mean rms
Harmonic voltage		
(refer to Table 6)		95% of 10 min. mean rms in 1 week
EVENTS		
Flicker, long-term severity		
$P_{lt} \leq 1$		95% of the time in 1 week
Voltage unbalance		
0% U_n to 2% U_n		3-phase, 95% of 10 min. mean rms in 1 week
0% U_n to 3% U_n		1-phase or 2-phase, 95% of 10 min. mean rms in 1 week

The EN50160 standard makes the distinction between continuous phenomena and voltage events. It considers that continuous phenomena are deviations from the norm

occurring continuously over time. The norm regards voltage events as sudden and significant deviations from the standard, attributed to faults and weather conditions that are unpredictable. This distinction is made in the tables. The separation of variations into these two groups leads to the type of measurement method that should be used to detect and measure the phenomena. While stationary phenomena need to be continuously monitored, non-stationary phenomena need to be detected by some type of triggering method because they are generally fast and non-repetitive in nature [4].

Harmonic voltage is defined as a sinusoidal integer multiple of the fundamental frequency, while inter-harmonic voltage is defined as a sinusoidal voltage that is not an integer multiple of the fundamental frequency. Harmonic voltage is to be measured over a period of one week. 95% of the 10 minute mean rms values for the individual harmonic components must be less than those indicated in Table 6 [1].

Table 6 - Harmonic component limits.

Odd harmonics multiples of 3		**Odd harmonics** not multiples of 3		**Even harmonics**	
Order (h)	**Rel. Voltage** (U_n)	**Order** (h)	**Rel. Voltage** (U_n)	**Order** (h)	**Rel. Voltage** (U_n)
3	5.0 %	5	6.0 %	2	2.0 %
9	1.5 %	7	5.0 %	4	1.0 %
15	0.5 %	11	3.5 %	6...24	0.5 %
21	0.5 %	13	3.0 %		
		17	2.0 %		
		19	1.5 %		
		23	1.5 %		
		25	1.5 %		

The total harmonic distortion (THD) that includes the first 40 harmonic components must not exceed 8% of the supply voltage. Harmonic components above 25 are not indicated as they can be small in value but are unpredictable.

2.2.2. Measurement Methods

Measurement aggregations over time intervals are also defined in the standards because the accumulation of data can be enormous. Statistical data that represents a parameter over a long period of time is easier to comprehend. Generally measurements are to be done over a 10 cycle period on 50Hz systems and over a 12 cycle period on 60Hz systems, both represent a 200ms period. These values can then be aggregated into larger periods of time where the most important ones are identified to be 3s, 10 min. and 2h. The algorithm used for measurement aggregation is defined as being the square root value of the arithmetic mean of the squared input values, but these exclude the method used for measuring flicker [13].

The clock deviation of the device is also defined as a clock-time uncertainty that should not exceed one cycle of the fundamental frequency. A time tagging tolerance of 1 s per 24 h is allowed when the monitor loses synchronization with an external clock signal.

A flagging concept is also indicated for use to prevent a disturbance from being identified as more than one parameter at the same time. If magnitude were to start dropping below the rapid voltage change limit, for example, a dip would be identified. A flag indicating that a dip had been detected should be set. If the magnitude were to continue to drop until it went beyond the maximum dip limit, an interruption is detected and its respective flag should be set. There is a problem however; the phenomenon should not be simultaneously identified as a dip and an interruption. The dip flag should be reset because in fact the phenomenon detected and measured is an interruption [13].

Methods for measurement of rapid voltage changes, considered to be quick transitions in rms voltage between two steady-state conditions are indicated. Thresholds should be defined for minimum rate of change, minimum duration of the steady-state conditions, minimum difference in voltage between the two steady-states and the steadiness of the steady states. The voltage in a rapid voltage change should not exceed the lower limits for both voltage dips and voltage swells. The basic measurement for voltage dips and voltage swells requires that the voltage is refreshed at every half-cycle $U_{rms(1/2)}$. The residual voltage is then considered to be the remaining voltage from the supply. The depth and the duration are also identified. The same method is to be used for interruption measurements. Overvoltage and transient overvoltage can be measured at any time, when they appear. The measurement for inter-harmonic components is not yet defined. Even at low levels these can give rise to flicker. Mains signalling should be measured on a daily basis and should be within limits defined in Figure 5.

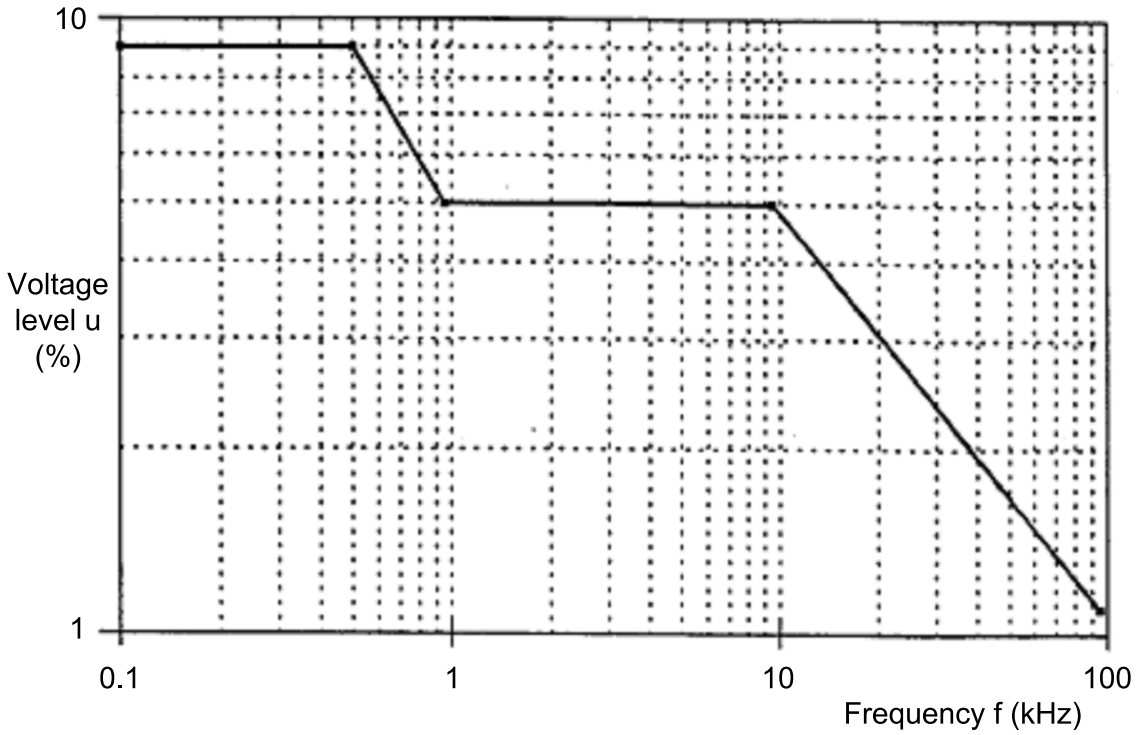

Figure 5 - Limits defined for mains signalling [13].

The method should verify the amount of signal for a known carrier. Measurement of other mains signalling where the base carrier frequency is above the limits indicated in this standard is referred to EN61000-3-8.

Voltage frequency should be measured over 10s periods. If the number of cycles is not a complete integer of the 10s window, the integral cycles included in this period should be used to determine the frequency. Before each assessment, harmonic and inter-harmonic components should be attenuated to minimise their effect on the fundamental frequency measurement and minimise multiple zero crossings. Measurement time intervals are not to overlap, with individual cycles that overlap having to be ignored. Each 10s clock interval is to start at an absolute 10s interval with a tolerance of ± 1 cycle in both frequency systems [13].

Magnitude is to be verified during a period of one week in periods of 10 min. The rms value of the voltage must be measured over a 200ms interval for both frequency systems. Every such interval must be contiguous, but not overlap and adjacent to the next interval. The rms value must include harmonics, inter-harmonics and mains signalling among others.

Unbalance is measured over a period of one week and is evaluated by the method of symmetrical components. In addition to the positive sequence component at least one of the other two components must exist, the negative sequence component or the zero sequence component.

Harmonic components will be measured during the period of one week in 10 min. intervals and will be verified according to the limits defined. The total harmonic distortion of the supply voltage including harmonic components up to order 40 must be equal to or less than 8% of the nominal supply [1].

2.3. Commercial Monitoring Systems

Portable power quality meters are now easier to find on the market compared to the earlier years of power quality monitoring. The development of rechargeable batteries in very recent years has also been a good contributor to this. Such tools can be acquired from almost any of the test instrument manufacturers in the world. The investment is still rather high even for most industrial end users.

Two devices were analysed to better understand the measurement capacities of such instruments as well as their characteristics. Both units are close to top of the range within their makes. The first unit is from a North American company, Fluke. The second unit is from a French company, Chauvin Arnoux. Their model numbers are 435-II and C.A 8335 Qualistar Plus respectively. They are identified as being a Three Phase Energy and Power Quality Analyzer and a Three-phase Electrical Network Analyser respectively.

Table 7 summarizes the parameters that were compared between the two monitoring devices: a) European standards; b) samples per cycle; c) sample resolution; d) sampling frequency ; e) input range; f) frequency measurement window; g) frequency resolution; h) how peak value for magnitude is obtained; i) how rms value for magnitude is obtained; j) how ½ wave rms value is obtained; k) how fundamental frequency and harmonics are measured; l) how harmonics are averaged; m) THD calculation; n) up to which inter-harmonic is measured; o) which flicker measurements are made; p) flicker resolution; q) flicker accuracy; r) how dips are measured; s) how swells are measured; t) how mains signalling is measured.

Table 7- Comparison between two monitoring devices.

	Fluke 435-II	Chauvin Arnoux C.A 8335
EN 50160	✓	×
IEC 61000-4-7	✓	✓
IEC 61000-4-15	✓	✓
samples per 50Hz cycle	500	256
sample resolution	40µs	78.125µs
sampling frequency	25kHz	12.8kHz
nominal input range	3Vp-p	1V
frequency measurement	10s (IEC 61000-4-30)	7 pos. zero-crossings
frequency resolution	0.001Hz	0.01Hz
peak value measurement	absolute	average
rms value measurement	10 cycles (IEC 61000-4-30)	--
½ wave rms value	average (10 min.)	max. & min.

measurement		
fundamental frequency & harmonics	FFT (IEC 61000-4-7)	16 bit FFT / 1024 samples
harmonic average	10 min.	(IEC 61000-4-7)
THD calculation	≤ H40 or ≤ H50	= H50 + 2nd distortion factor
inter-harmonic measurement	order 50 (IEC 61000-4-7)	--
flicker measurement	Plt, Pst, Pst (1 min.), Pinst (IEC 61000-4-15)	Plt, Pst (10 min.)
flicker resolution	0.01	--
flicker accuracy	± 5%	--
dips	½ wave rms	combined dips & interruptions
swells	½ wave rms	swells = surges
mains signalling	2 frequencies, programmable	--

Interestingly enough, the first refers to the European EN50160 Standard and analyses data against the parameters set by this standard but the second one, although mentioning the Standard does not analyse data against those parameters. The only references that are made by the latter one to any of the European standards mentioned is IEC 61000-4-15, where they indicate that the method for flicker measurement is based on that standard, and IEC 61000-4-7 to determine harmonic components [9].

Both instruments acquired the digital signal from a 16 bit analogue-to-digital converter. The first unit captures 500 samples for every 50Hz cycle, each 40μs wide while the second captures 256 samples for the same cycle, each 78,125μs. Their sampling frequencies are thus 25.000Hz and 12.800Hz respectively [5].

The nominal input range of the first device is 3V peak-to-peak and has a fixed and a variable scaling factor up to 10.000:1, while the second device has a nominal input of 1V.

For the first, the frequency is measured over a 10s period as is defined in IEC 61000-4-30 and has a frequency resolution of 0.001Hz. For the second, the frequency measurement is made by analysing seven consecutive positive zero crossings after digital low-pass filtering and removal of Direct Current (DC). The precisely measured zero crossing is obtained by linear interpolation of the two samples to reach a better resolution of 0.002%. This later device has a frequency resolution of 0.01Hz [5].

The absolute highest value is obtained for peak values in a 10 cycle interval with 40μs sample resolution for the first instrument. The second instrument seems to measure the positive peak and the negative peak then calculates an average.

For the first meter, root mean square values are calculated over 10 cycles that do not overlap with 500 samples per cycle as indicated in IEC 61000-4-30. The half-wave root mean square value is measured over one cycle and is calculated for every half-cycle according to IEC 61000-4-30. The measurement is averaged over a period of 10 min [9]. For the second meter, the half-cycle root mean square values are used and these maximum and minimum values too.

FFT algorithms according to the IEC 61000-4-7 standard are used to calculate the fundamental and harmonic components (up to order 50) of the input signal over a 10 cycle time window for the Fluke unit. The window is approximately 200ms but depends on the fundamental frequency. Phase locked loop algorithms are used to capture an exact number of cycles. Harmonics are averaged over a period of 10 min. Total Harmonic Distortion (THD) can be calculated for harmonic components up to order 40 or 50 [9]. The Chauvin Arnoux unit uses a 16 bit FFT with 1024 samples, which are 4 cycles, over four periods without windowing according to IEC 61000-4-7 to determine harmonic components. THD is calculated for harmonics up to order 50, a second distortion factor is also calculated with reference to the rms value [5].

The first apparatus measures inter-harmonics up to order 50 according to IEC 61000-4-7. The second apparatus does not mention inter-harmonics.

Flicker characteristics that are measured by the Fluke meter are: a) long-term severity, Plt; b) short-term severity, Pst; c) short-term severity over 1 minute; Pst (1 min.); d) instantaneous severity, Pinst; with a resolution of 0.01 and an accuracy of ± 5%. The measurement is done according to the design and functional specification for the flickermeter in IEC 61000-4-15. The measurement is averaged over a period of 2h. The flicker characteristics measuring method for Pst is inspired by the IEC 61000-4-15 standard over a period of 10 min [9]. The later unit measures Plt and Pst (10 min.) inspired on the IEC 61000-4-15 standard [5].

Fluke uses the half-wave rms values for the detection of dips and swells that include the flagging concept according to the European Standard and the user can set the limits. Chauvin Arnoux uses a combined measurement for dips and interruptions and measures swells as if they are surges.

The first instrument detects transients on the half-wave rms values or instantaneous flicker severity (Pinst) by capturing the waveform triggered on a signal envelope. For this, the device has a bandwidth up to 100kHz [9]. The second instrument compares the cycle samples to those of the previous cycle signal envelope. As soon as a sample is outside the envelope, that cycle, the one before and the next two are pushed to memory. The device continues to use 256 samples per 50Hz cycle [5].

Fluke allows the threshold, limits and signalling duration for mains signalling to be programmable for two signalling frequencies between 60 and 2.500Hz and are averaged over a period of 3s. Chauvin Arnoux does not mention mains signalling.

Both units also have measurements for voltage unbalance, transformer inrush currents and power related calculations like power factor with a resolution of 0.001and displacement power factor or energy metering.

Both instruments are good but there would be an obvious choice to use the Fluke meter as it is the one that more globally complete between these two units, it includes inter-harmonic measurement and time aggregation. The measurement options differ where

the first model allows for overall monitoring. It would be unfair not to mention that there are other devices from several other manufacturers also on the market. This comparison demonstrates that each manufacturer has a different philosophy when it comes to power quality monitoring. These two apparatus were compared because they were more at hand.

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3. Signal Processing Units

This chapter will describe the modules implemented for processing the power signal and obtaining the correspondent power quality parameters. The input signal for processing is considered to be the output of an analogue-to-digital converter. As explained in Introduction, it will be assumed that the analogue signal is properly conditioned before it is converted to the digital domain, as shown in Figure 6. The analogue anti-aliasing filter must be used to remove the high frequencies that are not relevant to avoid confusion with the lower frequencies to be measured to be then converted into a digital signal [10].

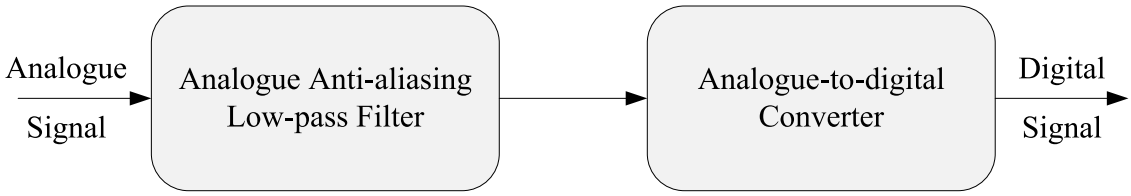

Figure 6 - The pre-processing stage of the signal.

Before the digital signal analyser can be designed, careful consideration is necessary to decide what sampling frequency should be used to sample the input signal. Figure 7 shows an overview of the compromise between sampling frequency, resolution and hardware resources.

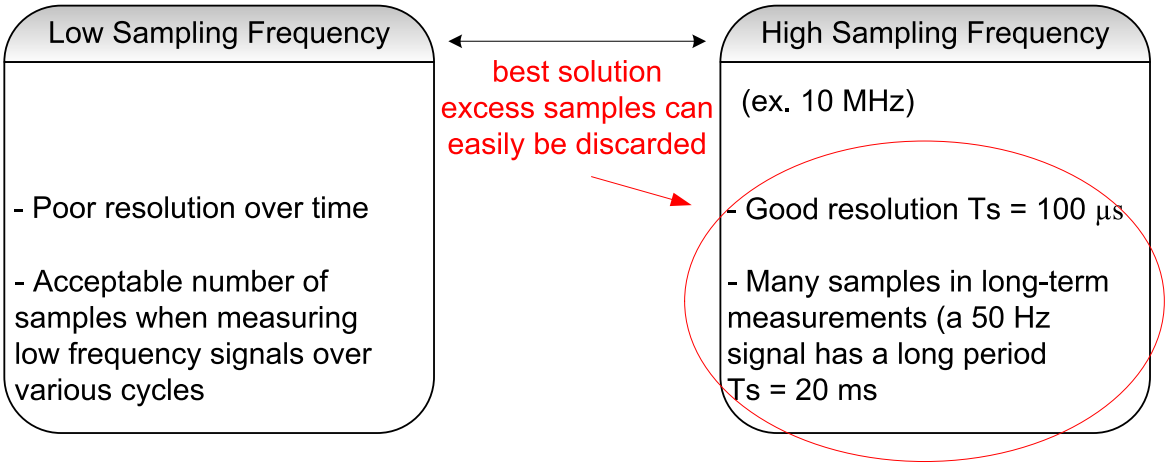

Figure 7 - Overview of trade-offs regarding the chosen sampling frequency.

The sampling frequency will define the maximum resolution of measurement for the system but there is a trade-off. For low sampling frequency poor measurement resolution will prevail over time. There will be an acceptable number of samples for measurements of low frequencies while high frequency measurement will result in very few samples. For a very high sampling frequency for example 10MHz, the resolution will be very high with a sampling time Ts = 100ns. The fundamental frequency of 50Hz, which is what is to be expected, has a full cycle of 20ms. An enormous amount of samples would have to be

stored if post-processing is required over one or several cycles. Still it is a better solution as excess samples can always be easily discarded.

Figure 8 shows the overall simulation process that was to be used. Input signals would have to be used to stimulate the inputs of the FPGA models and their outputs would then have to be verified for accuracy.

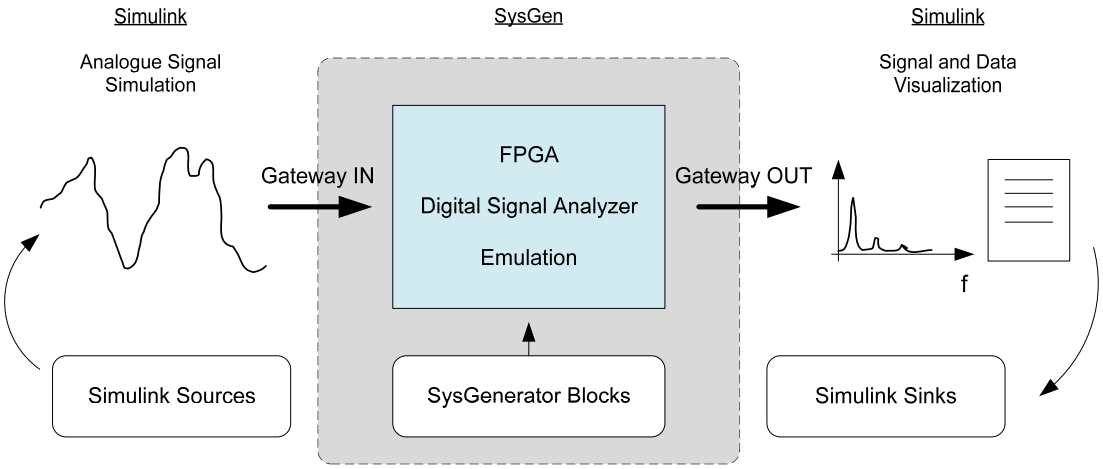

Figure 8 - The simulation overview.

All the expected input signals were to be simulated with Simulink sources. Composite signals would be created with the Simulink building blocks. These included the nominal magnitude and frequency of the signal with no disturbances. It included variation disturbances such as frequency deviation and magnitude deviation, harmonic distortion, inter-harmonic distortion and mains signalling. It also included events such as dips, swells, transients, interruptions, noise, flicker and waveform distortion.

The FPGA digital signal analyser was designed at the lowest abstraction level possible, the hardware level. The circuits were constructed with the aid of a system generator graphical tool by placing blocks together and emulated to obtain the required results. Several algorithms were implemented in the FPGA to obtain different power quality parameters. To implement these algorithms, all the usual issues related to hardware implementation had to be considered, such as the number of bits used to represent each sample, their format (signed or unsigned), synchronization issues, processing latency, hardware resources for storing and processing data. Information was extracted from the input signals so that decision-making could be possible, values were accumulated and divided to obtain average and root mean square (rms) values. Various other functions were used such as accumulation, division and bit manipulation. Feedback loops, filters, detectors, memories, delays and registers were also used [18].

The interfacing between Simulink signals and system generator DSP signals were done through the gateway ports, one dedicated to inputs and the other dedicated to outputs.

The digitally processed signals were analysed with Simulink sinks. Values were sent to displays for verification or to workspace memory to be exported or plotted. Scope

displays were also used to analyze the signals, triggering moments, impulses and magnitude values.

The macroscopic architecture of the implemented digital signal processing unit is given in Figure 9. After the pre-processing phase, the signal processing is divided into two types of signals; a) stationary signals, where gradual deviations are monitored; b) events, where sharp deviations are detected. The features of the power quality parameters are extracted so that their correct classification can be made.

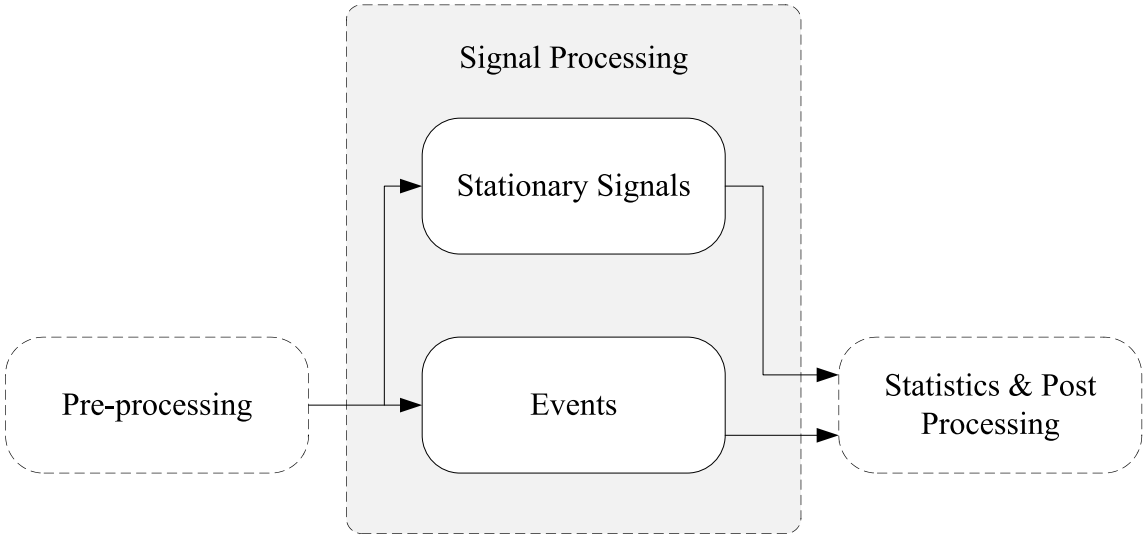

Figure 9 - Signal processing architecture.

The signal processing unit is divided into two distinct modules: one for analysing stationary signals and the other for analysing events. As this is a hardware implementation, both modules are expected to be working in parallel.

Stationary signal variations were those that needed to be continuously measured over time due to their gradual deviation in nature. Generally these measurements can be taken as average values over a window of time such as a 10-cycle window, a very common time period used in power quality analysis [10]. In this implementation, this measurement time window is also possible, as well as, being able to access data for every cycle.

On the other hand, events are considered to be exceptional occurrences, generally of large deviation in nature and possible at any instant in time. Thus, they need to be registered and classified correctly [10]. In this implementation, a monitor has been implemented to detect events and allow the system to save the measured data for post processing analysis.

In the following sections, each of these modules will be described in detail. Design requirements will be described, as well as implementation issues and trade-offs. Section 3.1 is devoted to the modules responsible for processing stationary signals, section 3.2 describes modules used for data aggregation and site indices calculation and, finally, section 3.3 describes the modules related to events.

3.1. Processing of Stationary Signals

Figure 10 shows the proposed overall architecture of the implemented stationary signal processing module. This module includes data processing blocks (white blocks) and data post-processing blocks (grey blocks). The white blocks are responsible for obtaining measurements while the grey blocks are responsible for data analysis and aggregation.

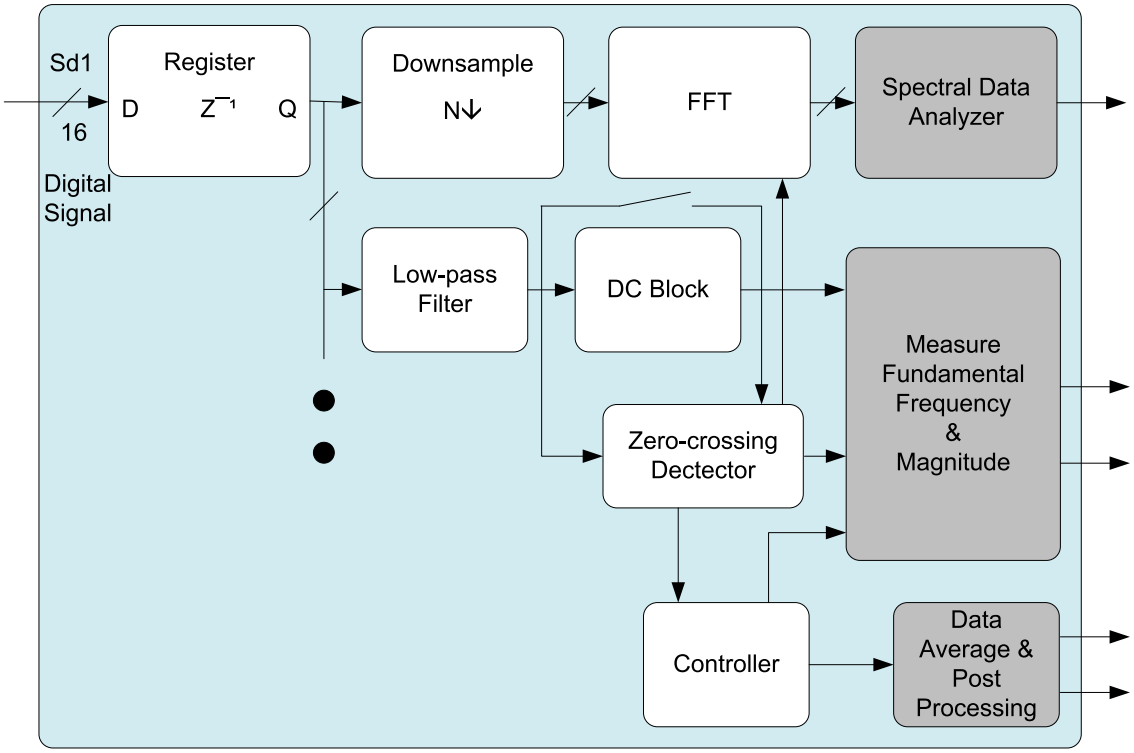

Figure 10 - Stationary signal processing unit architecture.

After signal synchronization with the hardware clock, the signal is then split into two separate paths: the first one dealing with the measurement of frequency harmonic and inter-harmonic components; and the second one dealing with the measurement of the fundamental frequency, its magnitude and its direct current (DC) average value.

The method chosen to acquire information on the harmonic components was the use of the Fast Fourier Transform (FFT), a faster version of the Discrete Fourier Transform (DFT). It is a mathematical algorithm used to decompose a signal into its various components over the frequency-domain. In this context, frequency components are usually classified as harmonic and inter-harmonic components. The fundamental frequency of the signal would always be the first of the harmonic components. This method was chosen as it is widely used for this process with success, becoming an important part in this project.

The signal was down-sampled before it was placed at the FFT. The effect that this down-sampling had was the lowering of the sampling frequency which lowered the computational demands on the Fast Fourier Transform. Each frequency bin footprint at the

FFT output became narrower which meant that the magnitude measured at each bin represented a smaller frequency band. This will be explained in greater detail in section 3.1.1.

A spectral data analyser was then used at the output of the FFT to separate the harmonic and inter-harmonic components from each other. These values were then averaged over predetermined time periods in a time aggregation process as defined in the European Standard EN50160 [4].

In the second signal path, a moving average low-pass filter was used to remove high frequency noise from the signal. It was used to smoothen the input signal, helping to eliminate the undesired detection of false zero crossings, due to additive noise.

The signal was then conditioned with a DC block. Here, any direct current that could influence the reference axis of the signal was removed by blocking it. The positive peak value of the signal was compared to the negative peak value of the signal. The difference in their magnitudes indicated the DC component that was superimposed on the alternating waveform.

A zero-crossing detector was used to detect each time the signal crossed the value of zero. Both the transitions from positive to negative as well as from negative to positive were detected. These detections were needed for synchronization purposes of other sections.

The fundamental frequency and magnitude measurement block measured frequency, positive and negative magnitude and calculated the root-mean-square equivalent value. All these values were measured per cycle. An additional value was calculated: the half-wave root-mean-square value for every half-cycle.

In the following subsections, these blocks will be explained in more detail.

3.1.1. The Fast Fourier Transform

Although the European Standard EN50160 only includes harmonic components up to order 40 for the calculation of Total Harmonic Distortion (THD), it does note however that this limitation is only conventional. The choice of the highest harmonic order to be measured would directly affect the choice of the sampling frequency to be used.

The highest frequency component being measured is called the Nyquist frequency. In a worst-case scenario it should never be larger than half of the sampling frequency. All frequencies measured that are higher than half the sampling frequency will appear as lower frequency components in the frequency range. This will cause incorrect interpretations of the data, therefore need to be eliminated.

The Discrete Fourier Transform (DFT) converts N points of the input signal into two N/2+1 points to its output. The input is known to be in the time domain due to the common

approach of signal entering into the DFT being samples taken over time. These are transformed into the frequency domain described as amplitudes of sine and cosine waves. The transform is done from polar notation into rectangular notation where the cosine wave represents the real part and the sine wave the imaginary part of the value. The signal at the input goes through a process of decomposition or forward DFT. The number of samples N in the time domain can be any positive integer, normally in powers of two because the FFT normally works with these.

To be able to get the system to be as accurate as possible in its measurements of all parameters, especially those involving fundamental and harmonic frequencies, a high sampling frequency would have to be chosen. The ideal would be to have the sampling frequency to be a multiple integer of the frequency being measured. Since the frequency being measured can vary, this condition is not always possible to guarantee. The largest frequency to be measured, taking into account that the decision was made to cope with harmonics up to order 50, would be 2.500Hz. This meant that the sampling frequency had to be higher than 5.000Hz to avoid the effect of aliasing. Aliasing is the effect that a frequency that is higher than half the Nyquist frequency appears as a lower frequency component in the frequency spectrum. Also to include the reserved frequencies used for communication over the grid by the network operators, a frequency that goes up to 9.000Hz, the minimum sampling frequency should be at least 18.000Hz. If this value should be used as the sampling frequency it would mean that 360 samples were necessary but the closest value in powers of two was 512. The sampling frequency should be equal to the product of the 512 samples and the 50Hz fundamental frequency to be measured, which is 25.600Hz. 10.24 samples would be available for each 2.500Hz wave cycle.

The resulting frequency bin footprint size or the resolution of the FFT was also taken into careful consideration. The standard indicates that each inter-harmonic component should have a frequency bin of approximately 5Hz to comply. Were it possible to choose the amount of samples per cycle to be multiples of the decimal number system, it would be possible to obtain frequency bin widths of 1Hz exactly.

If a sampling frequency of 1MHz was chosen for example, it would mean that a new sample was available at every 1μs. Each full cycle of a 50Hz signal would be represented by 20.000 samples, resulting in high resolution indeed. Since the processor is still 100 times faster than this, enough time was available for even the most complex of tasks, like calculations of a square-root of a number.

In an attempt to find the best solution for ultimate accuracy in the frequency measurements, various calculations were made. The results were drawn up into Table 8. The amount of samples is shown for each sinusoidal cycle, in this case 50Hz. The time available for each sample indicates the resolution possible for a measurement with that amount of samples per cycle, more samples will increase resolution. Since the measurements for harmonics were expected to be up to order 50, the amount of samples for that frequency cycle was also calculated. The variation for each case at 50Hz and 2500Hz was calculated both as a percentage and as a frequency value.

Table 8 - Number of samples versus resolution.

amount of samples	sampling time Ts	samples @ 2500 Hz	Δ [%] @ 50 Hz	Δ [%] @ 2500 Hz	Δ [Hz] @ 50 Hz	Δ [Hz] @ 2500 Hz
128	0,00015625	2,56	0,78125	39,0625	0,390625	976,5625
256	0,000078125	5,12	0,390625	19,53125	0,1953125	488,28125
512	0,000039062500	10,24	0,1953125	9,765625	0,09765625	244,140625
1024	0,000019531250	20,48	0,09765625	4,8828125	0,048828125	122,0703125
2048	0,000009765625	40,96	0,048828125	2,44140625	0,024414063	61,03515625
4096	0,000004882813	81,92	0,024414063	1,220703125	0,012207031	30,51757813
8192	0,000002441406	163,84	0,012207031	0,610351563	0,006103516	15,25878906
16384	0,000001220703	327,68	0,006103516	0,305175781	0,003051758	7,629394531

Each column represents a new alternative as the number of samples was increased in powers of two for a reference signal of 50Hz. As the sample count grew, so the sampling time Ts for each sample became smaller. A decision was made to measure harmonic components up to order 50 instead of only 40. This would translate in the FFT having to deal with a frequency of 2500Hz at least. For the number of samples on the 50Hz signal, their equivalent number of samples for the frequency of 2500Hz was also introduced. As sampling time Ts decreased, so samples for the 2500Hz signal increased. The resolution percentages Δ[%] was calculated for cases at 50Hz and 2500Hz. Only for a count of 16384 samples was the 50Hz percentage resolution below 0.01% and the 2500Hz percentage resolution below 0.5%. The 50Hz percentage resolution in hertz Δ[Hz] was 0.00305Hz which was well below the 0.01Hz recommended by the European Standard. The logical choice was to use 16384 samples for the sampling of a typical 50Hz cycle at the input of the FPGA.

Although the system network frequency is always expected to be 50Hz, this value can vary with a variation in generator speed. A resulting 20ms cycle of a sine wave will correspond to this reference frequency. Should the frequency increase, the cycle will take a shorter time to complete. This means that a complete cycle, or an integer number of cycles, plus a portion of the next consecutive cycle will be used in the FFT conversion. When the frequency decreases, the cycle becomes longer. This means that an incomplete cycle will be used in the FFT conversion or an incomplete integer number of cycles. This would result in spectral leakage. Spectral leakage is the effect of neighbouring components of lower magnitudes appearing around the frequency component that is being measured because the sampled signal is not entirely periodic and a non-integer number of cycles are being sampled [2].

To avoid the measurement errors induced by spectral leakage, the number of samples used for the FFT conversion should correspond to an integer number of periods. The result would be that the spectral lines would coincide with the harmonic frequencies of the signal and no spectrum would be at the inter-harmonics. Because the input frequency is variable, it is not possible to always have a complete number of cycles in powers of 2. The solution would be to use a controller, like a buffer, that would allow a number of whole cycles to enter the FFT and complete the remaining number of samples with zeros until the FFT became full. In this way the FFT transform would always be done on whole integer

numbers of the cycle and no cycle would be lost. For a frequency of 50Hz, 10 cycles are exactly 200ms in length. Should the frequency decrease the waveform widens so less cycles could fit into the 200ms window. For a frequency of 46Hz, each cycle is 21.739ms, so only nine full cycles are possible during the 200ms. The additional samples would have to be filled with zeros. This is similar for the higher frequencies; more cycles will fit into the 200ms window. This was not implemented, but it could have been.

The harmonic and inter-harmonic component measurements were based on the Fast Fourier Transform block. It is a computationally efficient algorithm to calculate the Discrete Fourier Transform for sample sizes in integer powers of 2, in this case up to a maximum of 65535. The decision was taken to use at least two full cycles of the input wave for each transform, a total of 32768 samples. Figure 11 shows the Fast Fourier Transform pinout [19].

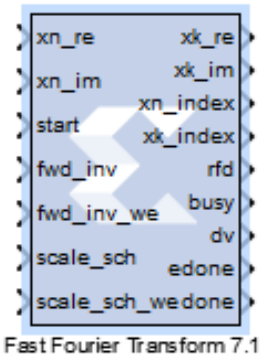

Figure 11- The Fast Fourier Transform Block used.

At the output, xk_index was used for the address position of the data available at the FFT outputs. Data valid (dv) was used to enable the FIFO buffer to clock in the data. The pulse available at edone which was active high one sample period before the FFT block was ready to output the processed data frame, was used for enable and reset purposes of other blocks within the circuit.

The FFT was started only after the first full cycle had been detected to allow its internal circuitry to stabilize after start-up. The digitized signal was placed at the real number input while zero was placed at the imaginary part of the input.

Initial results of the FFT for two full cycles and no down-sample produced a frequency bin footprint size of 25 Hz. The frequency bin footprint size had to be brought down. To divide the footprint by half, the down-sample had to grow by a multiple of 2 each time. Therefore for the footprint to be only 1.5Hz wide, the down-sample had to grow up to 32. This was the value used for maximum accuracy. For every down-sample by a factor of two, the FFT would use twice as many cycles for the transform. The total amount of cycles needed increased to 64 resulting in an output available only after every 1.28s.

Figure 12 shows the configuration used for the FFT. The input samples are reduced before being allowed into the FFT. The bin number is obtained from the FFT output

directly but the magnitude module has to be calculated before both are available to the spectral data analyser. The raw data from the FFT block is also sent to memory so that it can be available for external processing.

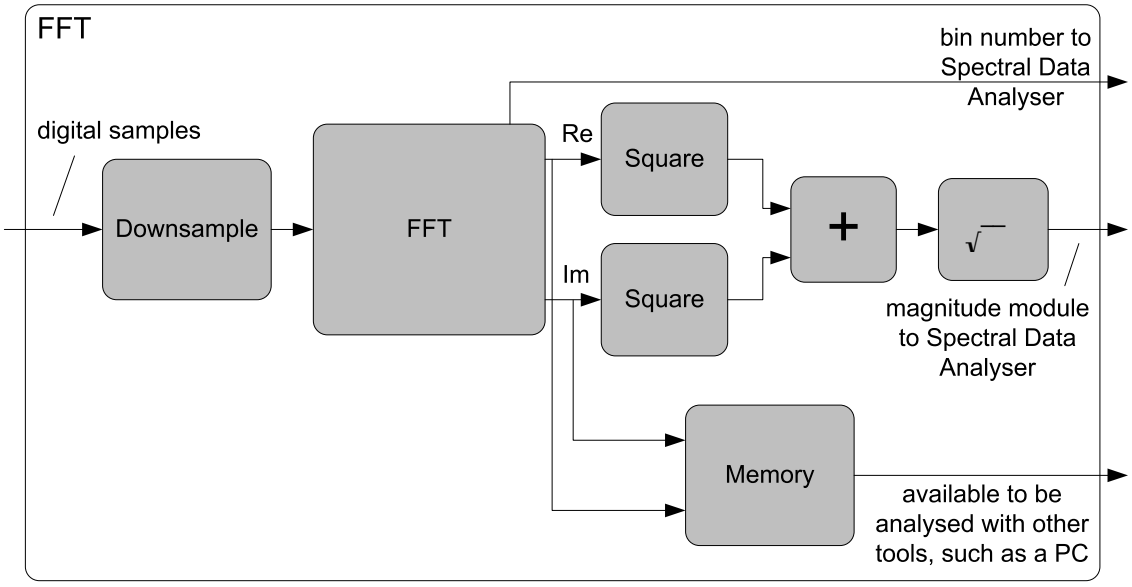

Figure 12 - The FFT configuration used.

The 16384 digital samples at the input were down-sampled by a factor of 32 before entering the FFT block. The resulting lower sampling frequency is directly proportional to the FFT frequency spectrum output on the x-axis. By maintaining the large FFT sample count for each transform at 32786, the number of bins was kept high. This combination resulted in high resolution of 1.5Hz per frequency bin. The frequency spectrum bin number was available directly from the FFT block output, while the magnitude was available as a complex value. To obtain the corresponding module for the magnitude corresponding to each bin, the complex values were squared, added together and then square-rooted.

The FFT output was also directed, with no modifications, into memory so that the raw data could be available for use with other processing methods such as through the use of a program on a personal computer. The implemented full system that includes the spectral data analyser is shown in Annex 1, 2 and 3. Annex 4 shows the FFT subsystem.

3.1.2. The Spectral Data Analyser

The Spectral Data Analyzer was used to find the harmonic components out of the range of complex data resulting from the FFT. Figure 13 shows the architecture of the implemented Spectral Data Analyser.

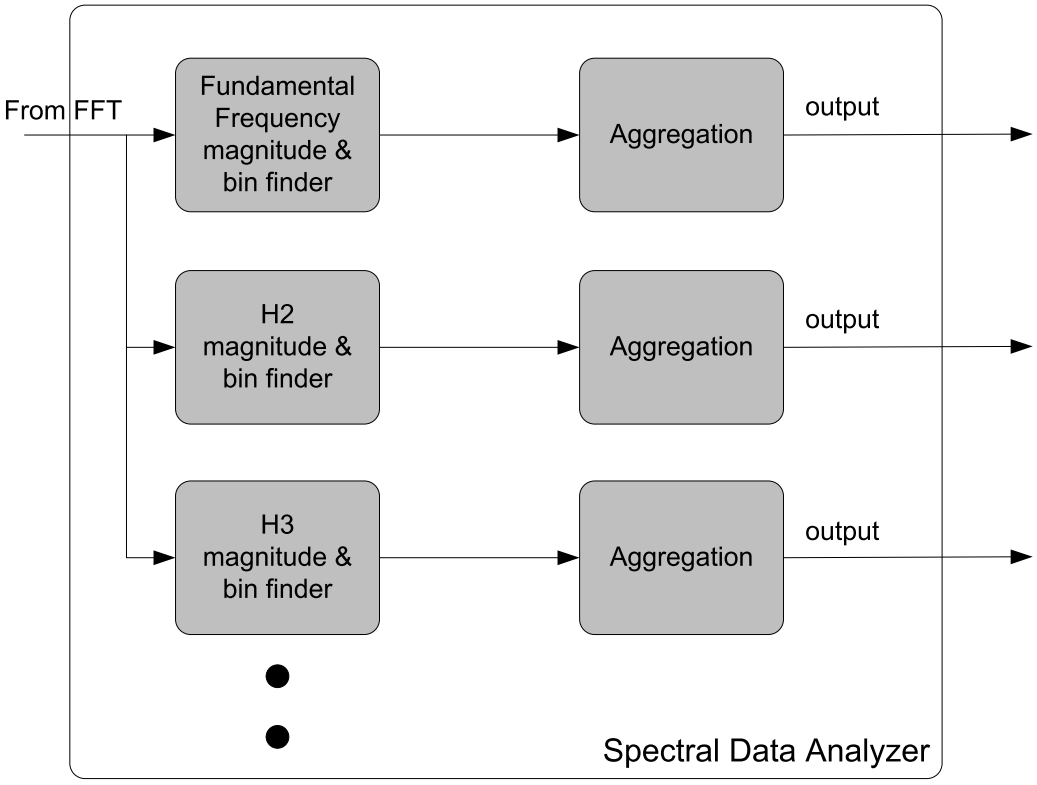

Figure 13 - Spectral Data Analyser architecture.

The first task that needed to be carried out was to find the bin number of the fundamental frequency. In our local power network, the fundamental frequency is expected be around 50Hz, but it can vary. A known fact about the fundamental frequency at the output of the FFT was that it would have the highest magnitude of all harmonic components. So, it was only necessary to find the highest magnitude - its corresponding bin number would be the fundamental frequency bin. By scaling down by a factor of 16384, the fundamental frequency magnitude was obtained. Care was taken to use only the positive bin numbers for the manipulation of this data.

Since the fundamental frequency was also the first harmonic component, to find the second harmonic component was fairly straight forward. The second harmonic component would be found at exactly twice the fundamental frequency. Simply multiplying the fundamental frequency bin number by two would result in the second harmonic component bin number, as was implemented. The corresponding magnitude value for that particular bin number was then used to obtain the magnitude of this harmonic component.

To obtain the third harmonic component frequency and magnitude, the process started by multiplying the fundamental frequency bin number with a value of three. The third harmonic component is always exactly three times the fundamental frequency. As before the corresponding magnitude value was found for that particular frequency. The same process would be used to find the other harmonic components.

Although the inter-harmonic components were not processed, the method used for their identification would be much the same as the one used to obtain the harmonic

components. Some of these values would need to be accumulated to present the result as a group of inter-harmonic components as indicated in the European Standard or, alternatively they could simply be available in this more raw state to the user.

Aggregation was done for the fundamental frequency, harmonic component two and harmonic component three as could also have been done for other harmonic and inter-harmonic components. Each respective value was accumulated when the data valid was true for the period of each aggregation.

Various timers were implemented, each for 200ms, 1s, 3s and 10s. For timers with larger periods, the process would just need to be followed in the same way. The first 200ms timer, autonomous in its time, would serve as the initial component. It was composed of a counter that would count 10 times more samples than those defined for each cycle, 163.840. Since each count reflected the time of each sample, the result had to be 200ms. The 1s timer would rely on this previous value to count it five times over. The 3s timer would count the 200ms timer result three times over. The 10s timer would count the 1s timer result ten times over.

During the 200ms aggregation periods, when the data was valid, the circuit would accumulate the value it was registering until the aggregation period was reached. Each time a new value was added, a counter would also be incremented. The total accumulated value would be divided by the value from the counter to find the averaged value over the 200ms. This value then became available to the 1s aggregation circuit that it in turn became available to the 3s and the 10s aggregation circuits.

There was a problem however. Since the FFT needed 64 complete cycles to process each time and each cycle was expected to be 20ms, a new FFT output would only be available at every 1.28s. A trade-off would have to be made between FFT output resolution and the amount of cycles needed for each transform. The FFT would have to work with 10 cycles to present a new output at every 200ms. The down-sampling was brought down to 5 and the FFT transform kept at 32768, the result was a frequency bin footprint of 10Hz. It is feasible to have two Fast Fourier Transformations running at the same time; one with high accuracy returning a new value at every 1.28s and a second with less accuracy that complies to the aggregation standard time of 200ms. The implemented power spectral data analyser is shown in Annex 5.

3.1.3. The Low-pass Filter

The moving average filter is a very simple filter that is easy to implement. It is also a very common filter used in Digital Signal Processing (DSP). Despite it being very simple it is optimal for reducing random noise while retaining a sharp step response. Its operation is based on averaging a number of points from the input signal into each point for the output signal. It has a smoothing effect by decreasing the amplitude of the random noise which is good. The noise reduction is equal to the square-root of the points used for the average.

Figure 14 shows the configuration of the moving average filter used. It is implemented with 31 delay blocks which do the same as a shift register, 31 adders and a divider by 32. Note that this divider can be very efficiently implemented using a simple shift operation.

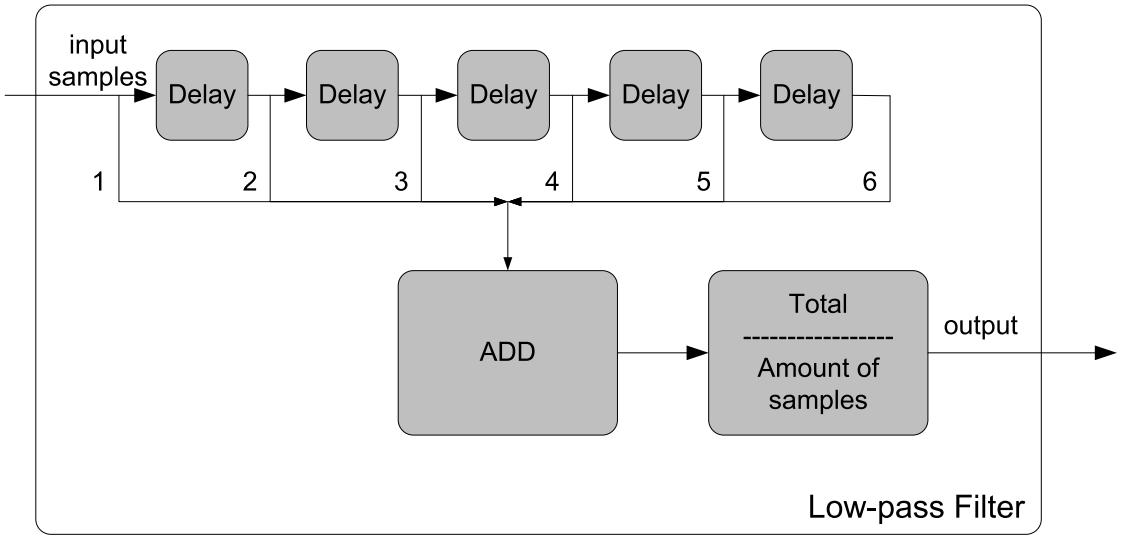

Figure 14 - The configuration of the moving average filter used.

In this case a 32 bit moving average filter was chosen which means that the noise would be reduced by a factor of 5.66. It is a good smoothing filter. No other type of digital filter is faster [17].

Other moving average filter relatives have better frequency domain performance. Multiple-pass moving average filters can be used where the input is passed two or more times through the moving average filter. The decision was made to use only a single pass through filter to avoid affecting the accuracy in measurement of the peak values of the signal [17]. The implemented circuit is shown in Annex 6.

3.1.4. The DC blocker

The AC input being measured, to be truly AC, has to be free of any DC component. This does not mean that this input waveform will never have the two superimposed. To measure frequency of a sine wave correctly, the wave should be equidistant from the zero reference line or else incorrect measurements will be made.

To block the DC component totally from the AC signal, it had to be removed. This was done by subtracting the detected DC from the input signal. Figure 15 shows the architecture of the implemented DC blocker.

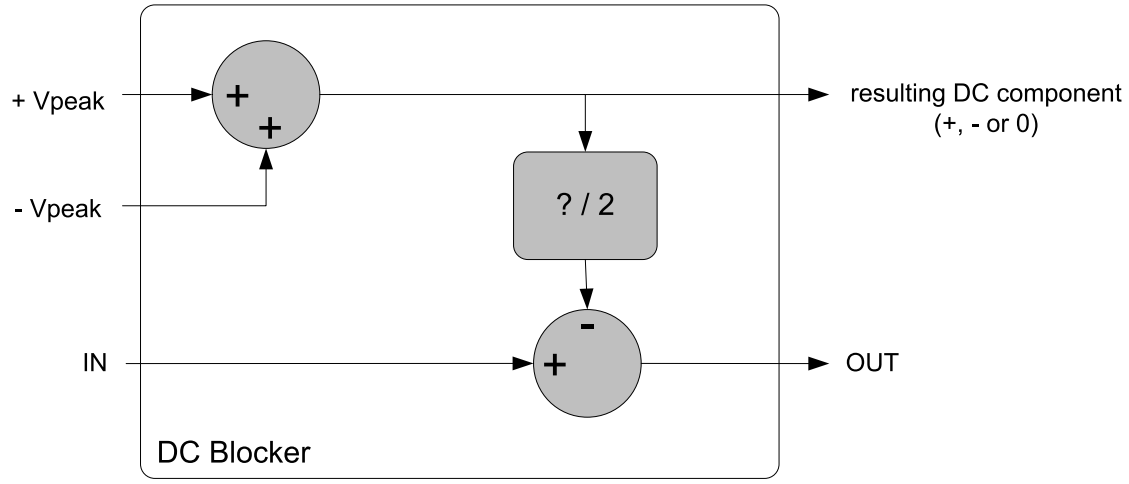

Figure 15 - The architecture of the implemented DC blocker.

To detect the amount of DC component present in the signal, the measured positive and negative peak magnitude were added together. If the resulting value was positive, positive DC had been detected and its magnitude would be immediately available as a result from this procedure. If the resulting value was negative, negative DC had been detected and again its magnitude would be available immediately. A result of zero would indicate that no DC component was present. The resulting DC component was divided by two before being subtracted from the input signal. This was done to avoid abrupt reactions to DC present for extremely short periods of time.

Synchronization of this section was done with the half-cycle and full-cycle information captured by the zero-crossing detector. Additionally, with a few more blocks, this circuit also indicated when the half-cycle was positive-going and when it was negative-going. The implemented circuit is shown in Annex 8.

3.1.5. The Zero-crossing Detector

The zero-crossing detector evaluated when the signal passed through zero in a transition from positive to negative and vice-versa. This was an extremely important tool in the system as it detected vital information like the end of each full cycle, used to synchronize various other blocks such as the FFT, the frequency and magnitude measurement block. This information has to be precise so that the measurements themselves can be as accurate as possible. The controller would also be able use this information should it be necessary.

Other information was also made available that was necessary for use in other blocks. These were both the detection of end of half cycle and that the half cycle was positive-going. Figure 16 shows the architecture used for the zero-crossing detector.

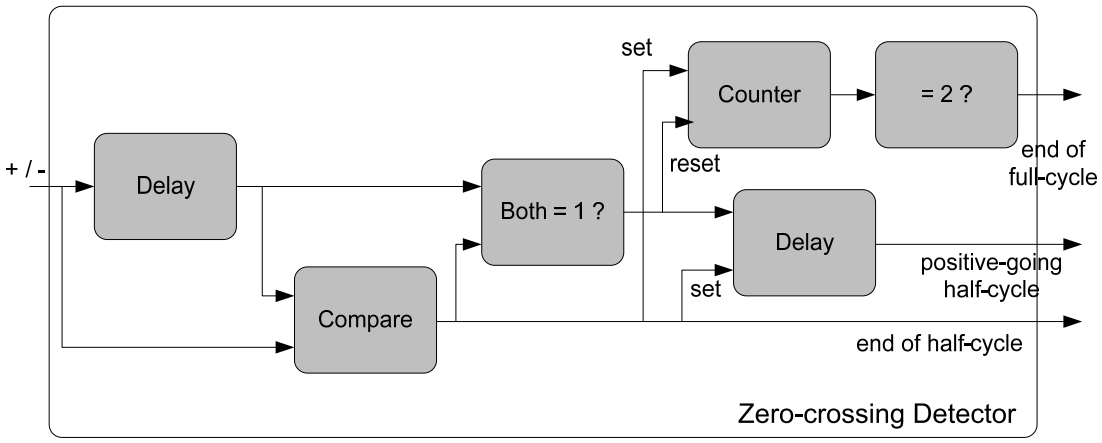

Figure 16 - The zero-crossing detector architecture.

The operation of the zero-crossing detector started by finding the sign of the present input sample it was then compared with the previous sample's sign. Should they be different, and end of half-cycle would be detected. This detection enabled a counter to count one value more as well as enabling the output for the positive going half-cycle, should that be the case. Should the value at the output of the counter be equal to two, the end of a full-cycle would have been reached and therefore detected.

If the previous sample was one, meaning that the signal was negative and going positive, the output of a logical and would cause a reset of the counter and would supply the value to the register that the half-cycle was positive-going.

If the previous sample was zero, meaning that the signal was positive and going negative, the output of the logical and would cause no reset of the counter and the value going to the register would be that the half-cycle was not positive-going. An inverter could have been placed here to indicate a negative-going half-cycle but it was not necessary.

This circuit was extremely accurate when detecting a negative to positive transition. But, when detecting a positive to negative transition, it delayed the zero-crossing half-cycle impulse by one sample, for the fact that when the sample was a zero, the sign was considered to be positive. Although detected in simulations, this will hardly be an issue in normal circuit operation because it is negligible. The implemented circuit is shown in Annex 7.

3.1.6. Fundamental Frequency and Magnitude

The fundamental frequency and magnitude measurement block performed three measurements on every cycle and calculated a fourth value. The values measured were the frequency, positive peak and negative peak values. The latter two were used to calculate the average DC equivalent otherwise known as the rms value.

Since the presence of harmonic components bring about deformity of the waveform but do not change the frequency at which the signal passes through zero, the frequency

measured will be the fundamental frequency. Figure 17 shows the architecture of the fundamental frequency measurement unit.

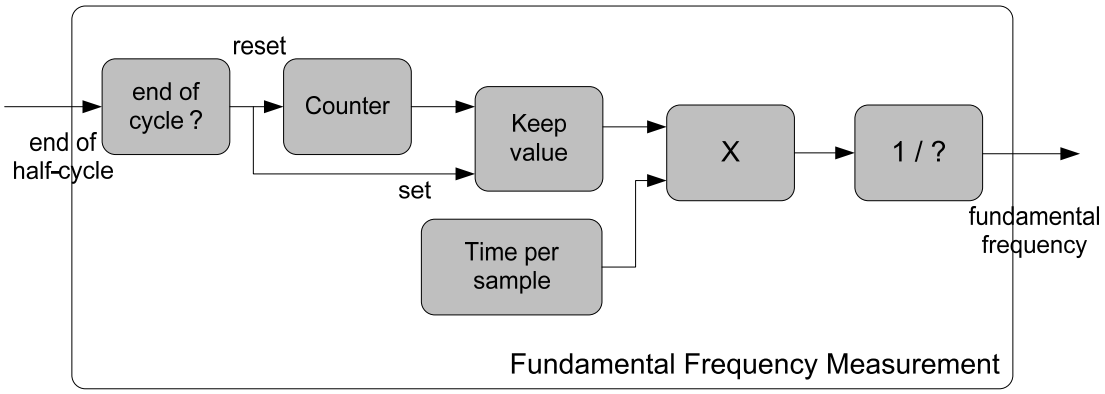

Figure 17 - The fundamental frequency measurement unit architecture.

To measure this fundamental frequency, the samples were counted from the beginning of a new cycle, from the moment the wave passed through zero, up to its end. This was supported on the synchronization with the zero-crossing detector. When the end was reached, the sample count was stopped and multiplied by the time of each sample. The value obtained was the total time the cycle took to complete itself. This value was inverted and hence, the frequency was found.

Figure 18 shows the architecture of the positive peak value measurement unit. To measure the positive peak value, each sample magnitude in the positive half-cycle was compared with the one before. Whichever was the largest was kept to compare with the next sample. The last highest value was the positive peak value. To make sure that this value was updated in the next positive half-cycle even if that peak value was lower, a reset of the value was done shortly after a new cycle started.

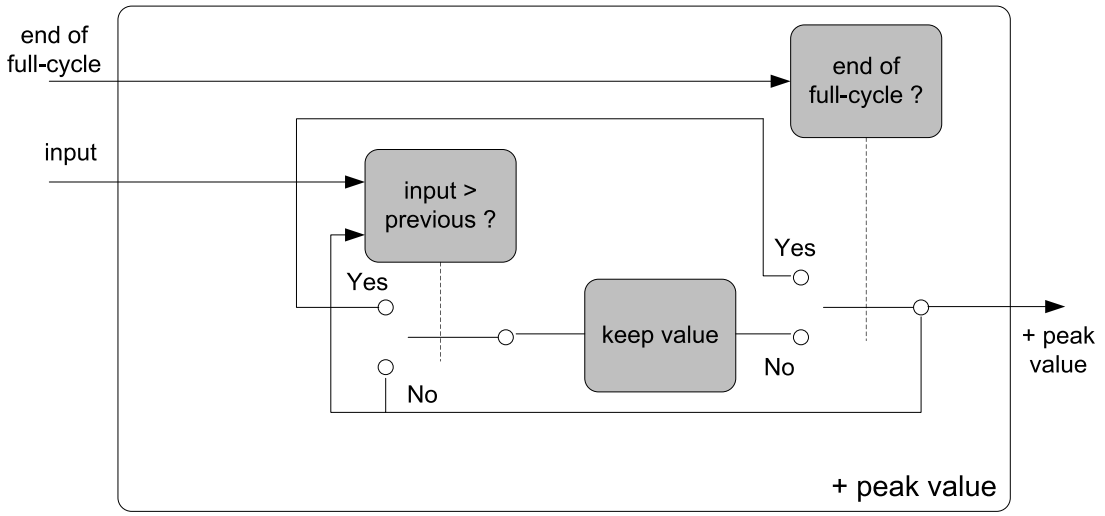

Figure 18 - The positive peak value measurement unit architecture.

Figure 19 shows the architecture of the negative peak value measurement unit. The negative peak value measurement was done in a similar way. The most negative value was kept to compare with the next sample. The lowest value was the negative peak value. Again, to make sure that this value was updated in the next negative half-cycle even if the peak value was more positive, a reset of the value was done shortly after the negative half cycle had begun.

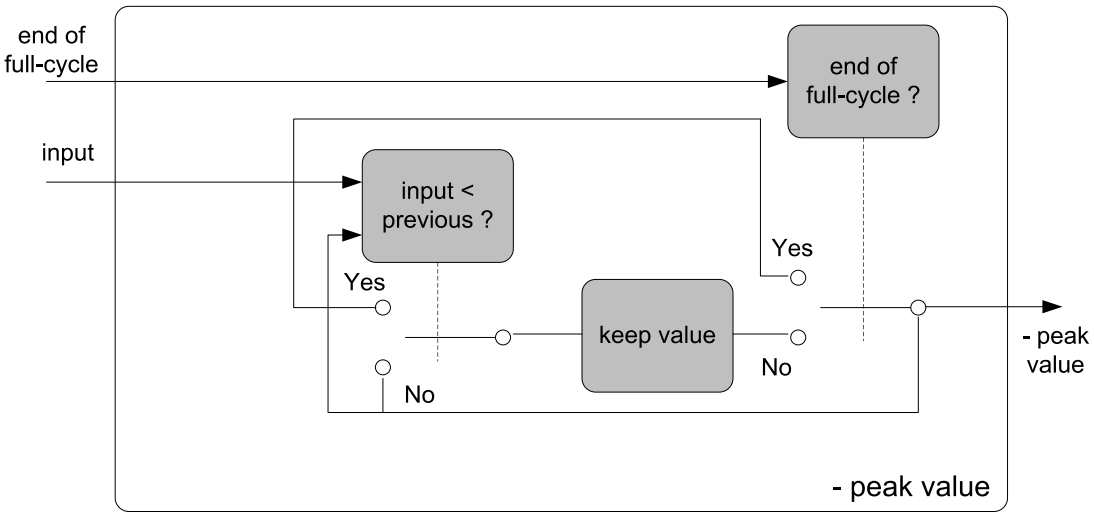

Figure 19 - The negative peak value measurement unit architecture.

Figure 20 shows the architecture of the rms measurement unit. The root-mean-square (rms) value was measured by squaring each sample. The value obtained was then accumulated to previous values belonging to the same cycle. When this procedure was completed for all samples of the same cycle, the total value was divided by the number of samples. The result was the average squared value for each sample. The square-rooted version of this value was the rms value. A second circuit was used to calculate the half-wave rms value. This later circuit would supply information to the processor when detecting waveform deformity so that the processor could know if the deformity occurred in the positive or the negative half of the input waveform. This value is also requested in the European standard.

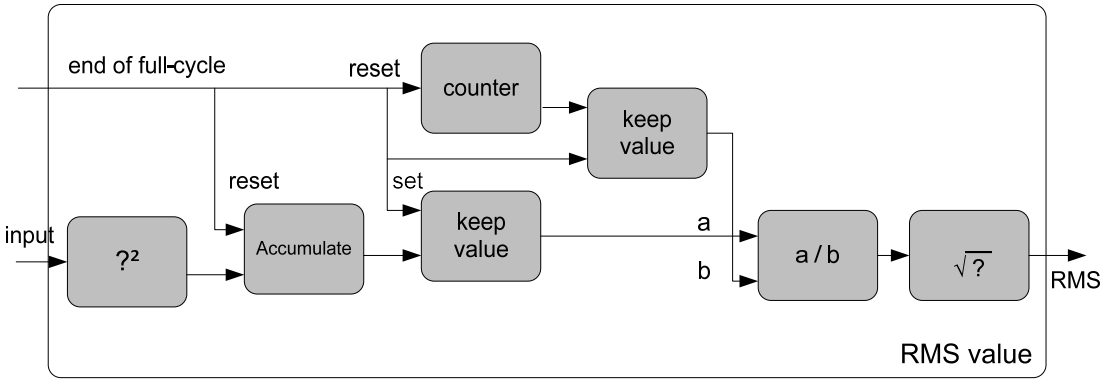

Figure 20 - The rms value measurement configuration used.

In each of the cases where a division was necessary, care had to be taken in its implementation. The output values were an integer result and a fraction, separate from one another. These two values had to be concatenated with each other and the decimal coma placed correctly in order to have a complete result with full integer and fraction.

A data valid was created for each of the four values so that other blocks could use this information accordingly. Aggregation of these four values was also done in the same way as in the Spectral Data Analyser. The values, fundamental frequency, positive peak value, negative peak value and rms were accumulated for 200ms exactly. It is worth noting that each of the values were initially measured for one wave cycle only, translating into maximum accuracy in the measurements and updated at every cycle. The implemented circuit is shown in Annex 19.

3.2. Processing of Events

To detect a sudden disturbance in the input signal such as a transient, a dip or a swell, various solutions are available, as the disturbances could be of extremely short duration, one or a few cycles long. Various methods are proposed by [10] for the analysis of non-stationary power quality events such as the use of wavelets or the Kalman filter. One other method would be to compare the present cycle with the one before. It would be a method rather difficult to use though. If the previous cycle was already contaminated with the disturbance, the difference between present and previous cycles could be negligible making it extremely difficult for accurate detection. An easier approach would be to compare the signal wave being evaluated against an ideal reference wave. This could be done with the use of a Phase-Locked Loop (PLL) to generate this reference signal.

After the synchronization of the input signal to the hardware clock mentioned before, signal processing of events could commence as is proposed in Figure 21. It includes the moving average low-pass filter, the DC block, the zero-crossing detector and the fundamental frequency and magnitude measurement blocks mentioned for stationary signal variations. It also includes the PLL block to generate an internal signal, a compare block to produce the difference between two signals and the threshold verifying block, explained

here. The data average and post processing, and the event identification blocks are also shown.

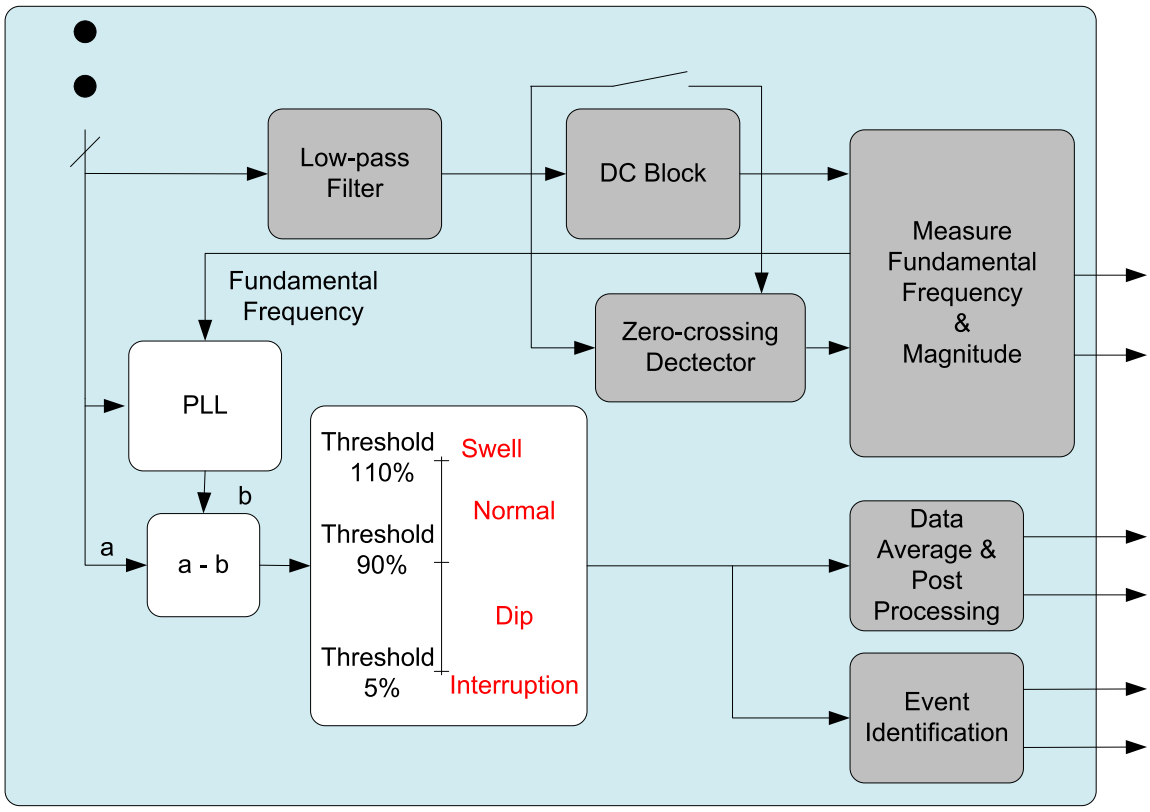

Figure 21 – Architecture of the event processing unit.

The Phase-Locked Loop (PLL) was the core on which the processing of events was based. It should assimilate the input signal with accuracy to generate its own sinusoidal output, which follows the mean input frequency. To implement this circuit in the digital domain, it is necessary to have an estimation of the nominal input frequency. Fortunately, this is readily available from the Fundamental Frequency Measurement block.

The comparison between the PLL input and output was made by finding the difference between the two waveforms. Although the processor could decipher the result, it would be possible for the hardware to set alarm flags for values above certain thresholds. Since the generated value was subtracted from the input signal, a positive difference above 0.08 (10 % of the input) would trigger the swell flag. A value between 0.08 and - 0.08 would have to be considered as normal under the European Standard. Any value between - 0.08 all the way down to - 0.792 should be classified as a dip while a value between - 0.792 and - 0.8 would be considered to be an interruption. The respective flags could be set in each of these cases. This information and the resulting error value can then be used by the processor to identify the type of event that may have occurred, along with information conveyed by previous blocks.

The implemented system is shown in Annex 18. Some blocks will be dealt with in more detail due to their complexity.

3.2.1. The phase-locked loop

As the name implies, the PLL is a feedback circuit that synchronizes its internal oscillator to the frequency of the input signal that it uses as a reference. If the two signals should differ, an error voltage generated within the circuit is applied to the oscillator to correct it so that the error will tend to zero. This loop continues until it locks itself on to the signal at its input. A generalized PLL block diagram is shown in Figure 22. The phase comparator (PC) compares the difference between phases of the generated signal with the input signal. The error is filtered by the low-pass filter (LPF) then fed to the voltage controlled oscillator (VCO) to adjust its output. So, the system continuously adjusts to the input.

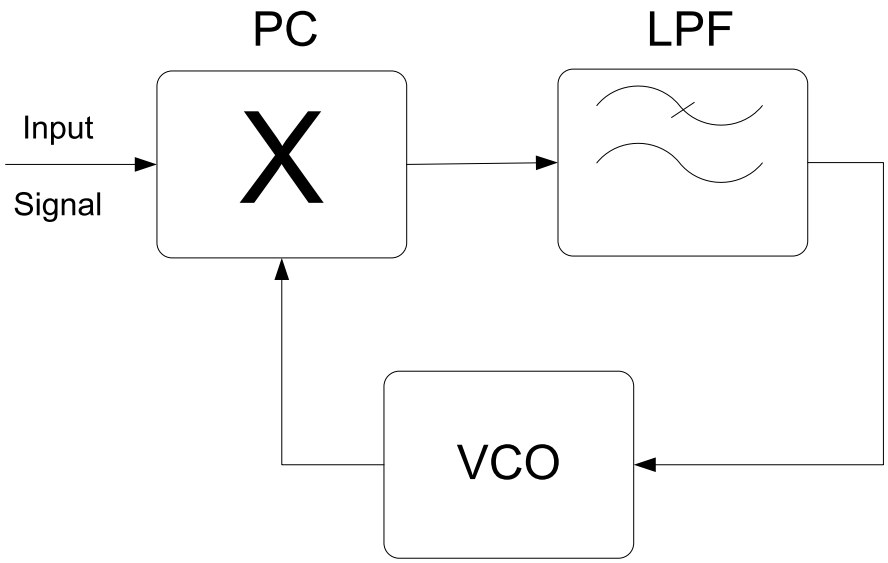

Figure 22 - The generalized PLL block diagram [7].

The PLL is frequency selective and designed to synchronize with the incoming signal despite the presence of noise. It is composed of three main sections; the phase detector, the loop low-pass filter and the voltage controlled oscillator (VCO). The phase detector compares the phase angle of the input signal with that of the signal output from the VCO. The resulting phase error is filtered by the loop low-pass filter that removes the high frequencies and noise. The resulting error voltage is the input control voltage for the VCO to adjust accordingly. A gain can be placed at the output of the VCO. The adjustments through the negative feedback circuit continue until the PLL frequency follows its input exactly. The ability for the PLL to self-adjust, after having locked onto the input, allows it to track the input frequency should it change.

To insure that the correct reference signals are generated for single-phase grid-connected systems, an orthogonal voltage system based on second order generalized integration (SOGI) can be used. The main task of this structure is to provide unity power factor operation, offering synchronization of current with the grid voltage. It uses a

transport delay block which is responsible for a phase shift of 90º with respect to the fundamental frequency [15].

A second-order generalized integrator could be used as the basis for the general structure of a single-phase PLL circuit [15]. The basic proposed PLL circuit is shown in Figure 23.

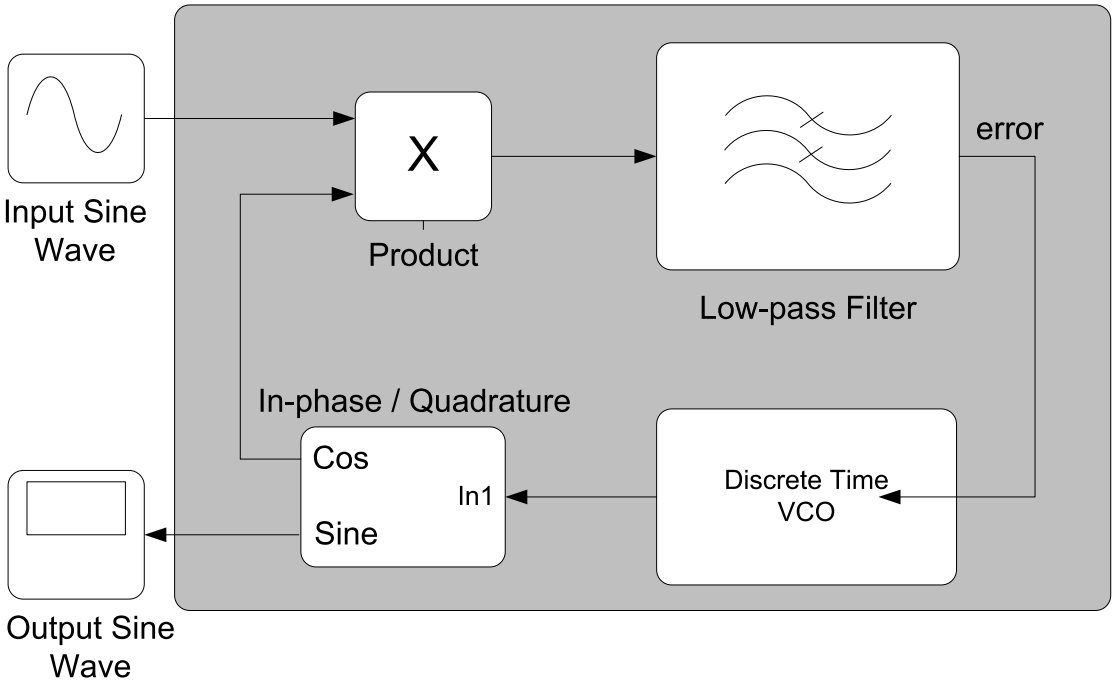

Figure 23 - Proposed PLL circuit.

The phase detection was done by multiplying the input with the generated cosine waveform from the in-phase / quadrature block. The resulting error waveform is fed through to the low-pass filter to remove the high frequencies and noise. The cleaned up error signal is used as the phase increment used at the input of the Voltage Controlled Oscillator (VCO). The VCO is an oscillator whose oscillation frequency is controlled by this external voltage which determines the instantaneous frequency of its output. When these control voltages are modulated at the input, phase modulation or frequency modulation is provoked at the output. The VCO, in turn, produces the sine wave with frequency to follow the input.

Figure 24 shows the phase-locked loop implementation in system generator blocks. The generated input is compared to the input signal with a multiplier block; this error value is fed to the finite impulse response (FIR) low-pass filter to cut off all high frequencies. The clean error value is input into the direct digital synthesizer (DDS), its output is sent to the second order generalized integrator (SOGI).

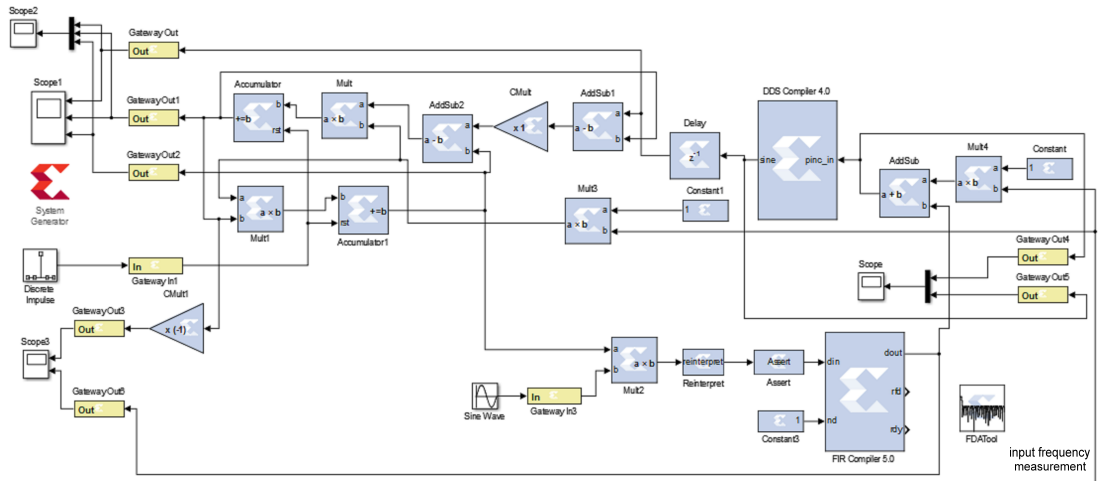

Figure 24 - PLL implementation.

The phase difference was achieved by multiplying the generated signal with the input signal in the first multiplier block. This resulting error waveform had twice the frequency and half the magnitude. The error was filtered by the low-pass FIR filter to produce the error voltage free from high frequencies and noise. A FIR filter is a filter whose input response is of finite duration; it settles to zero in finite time and generally lasts exactly N + 1 sample before going to zero. The error voltage was summed together with a nominal increment from the next time-instant step in the waveform, becoming the phase increment used at the input of the DDS. The DDS, in turn, produced the sine wave with frequency according to the input with a magnitude of one. The SOGI, composed of various blocks; delay, addsub, cmult, mult and accumulators, generated a sine wave and its cosine counterpart from the DDS output. The first integrator, adjusted by its gain, created a sine wave that was in-phase with the PLL input. The second integrator, adjusted by its gain, created a sine wave that was 90 º phase shifted when compared to the first integrator's sine wave. The cosine wave's phase was compared to the input phase in this closed negative feedback circuit.

In the implementation, although the output of the phase detector produced a waveform twice the input frequency and half its magnitude, the magnitude was still made smaller by using a reinterpret block. The loop low-pass filter order was kept as low as possible to reduce computational time. The FIR filter was setup with a sampling frequency of 1.500 Hz, stop frequency of 100 Hz and a pass frequency of 5 Hz to obtain a gradual cut-off ramp and a gain cut-off of 20 dB as shown in Figure 25.

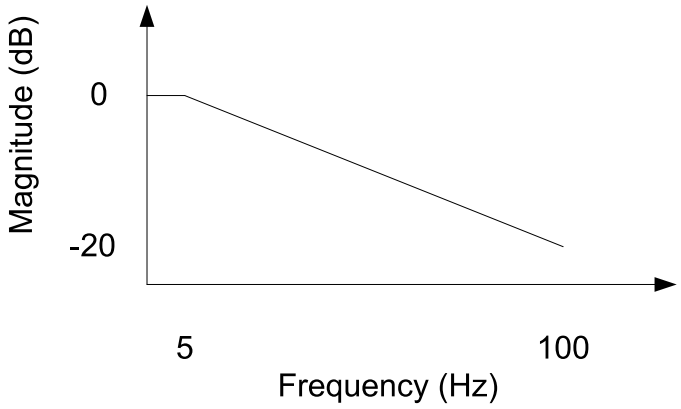

Figure 25 - FIR filter response.

A 100 Hz increase in sampling frequency or 5 Hz increase in cut-off frequency would increase the filter order by one. A two point increase could be observed when the stop frequency was lowered by 5 Hz. The output magnitude was also decreased with an increase in sampling frequency.

The phase increment added together with the error filtered from high frequencies from the FIR filter, were used as the control voltage at the DDS input block. A nominal increment of $T_s \times f$ was used instead of $2 \times \pi \times T_s \times f$ since the block used a normalised input, where T_s was the sampling frequency and f the frequency measured of the input. The DDS output was added to the first cumulative integrator output. This value was then added to the second cumulative integrator output to complete the feedback circuit. The adjusting constant used was $2 \times \pi \times T_s \times f$. The cumulative output of the first integrator was the sine wave that followed the input while the cumulative output of the second integrator, the cosine. Both the integrator inputs, before accumulation were multiplied by the adjusting constant.

4. Experimental Results

To verify whether the emulated Xilinx circuits actually worked inputs simulating real world scenarios were needed to do the experiments. Various circuits would be needed so that each situation could be simulated from the basic inputs to the stationary variations and events that the circuits should detect, to verify that all measurements were made correctly.

Due to the simulations done in System Generator being very heavy computationally, to obtain reasonable simulation times on the PC, resolution had to be brought down in the testing by reducing the sampling frequency. This has an obvious implication on the measurement resolution but this does not undermine the objectives which were to verify that the system constructed worked correctly.

Section 4.1 describes the test signals produced in Simulink to stimulate the system models, these are: a) the basic sine wave model; b) a dips and swell model; c) a frequency modulation model; d) a model for harmonic components; e) a model for noise; f) a model for transients. Section 4.2 indicates which values are measured at a site, implemented in System Generator while section 4.3 describes which frequency range make up the harmonic and inter-harmonic bandwidth considered in this project. Section 4.4 describes the implementation of event measurement and enumerates the events: a) dips and b) swells and other events. Test results are shown in these sections.

4.1. Test Signals

Test signal inputs could be generated in MATLAB by using equations that interpreted each signal mathematically. Simulink, doing the same but in a graphical interface would obviously be a better option because it becomes simpler for the user to use without having to know the underlying mathematical equations. This tool was chosen for the simulation of the real-life conditions.

Each system output should also be confirmed to conclude whether the system was working correctly or whether it needed any rectification. These outputs would also help in finding the source of the problems in the models should they arise.

Firstly, it was necessary to confirm that the Xilinx circuits were able to measure various characteristics such as the crossings through zero, frequency, positive peak and negative peak values and that the rms was calculated correctly. The most basic of models was needed to simulate the waveform resulting from the single-phase electric grid. This signal should be simulated as a discrete waveform as the input expected from the Analogue-to-Digital (A/D) converter would already be a digitized version of the analogue input signal.

The basic model of the sine wave was used as the foundation to elaborate the other more complex models.

4.1.1. The Basic Sine Wave Model

As mentioned, the simulation of the sine wave should be a discrete signal with enough samples for the Xilinx FFT to use as well as all the other blocks and subsystems. Signal quality should be sufficient to permit accurate measurements. A decision to have each sine wave cycle with 16.384 samples to be used by the FFT made the choice obvious. If the number of samples were even higher, the computational simulation would become heavier and slow down the simulation time even more. The sine wave should represent the input at the FPGA after scaling of the signal was done by the external circuits. The decision was made to use a magnitude of 0.8 as the reference to be equivalent to the input nominal value of 230 in a single-phase system so that a 25% margin would still be available for the detection of features such as swells. Since the frequency of the electric grid was expected to be 50Hz, this would have to be the frequency also used.

Such a block, the discrete sine wave, was available from the Simulink library DSP system toolbox where these parameters could be set, a block used for Digital Signal Processing (DSP) applications. The result was confirmed on a Simulink oscilloscope.

4.1.2. A Model for Dips and Swells

To simulate a dip in a sine waveform, the magnitude had to drop in the positive half-cycle and the negative half-cycle of the wave equally while the frequency was maintained unaltered. One way of doing this was to subtract another sine wave with the same frequency from it. It would also have to be in phase with the first one. The starting moment and the phenomenon's duration would have to be controlled so that the ultimate result was the original wave dropping in magnitude for the duration defined, then returning to its original value. A delay could be used for the launch of the second sine wave but its duration could not be controlled. The solution found was to use a switch that could be controlled with time, by controlling at which sample the switch would act, to start and another to stop the operation as seen in Figure 26.

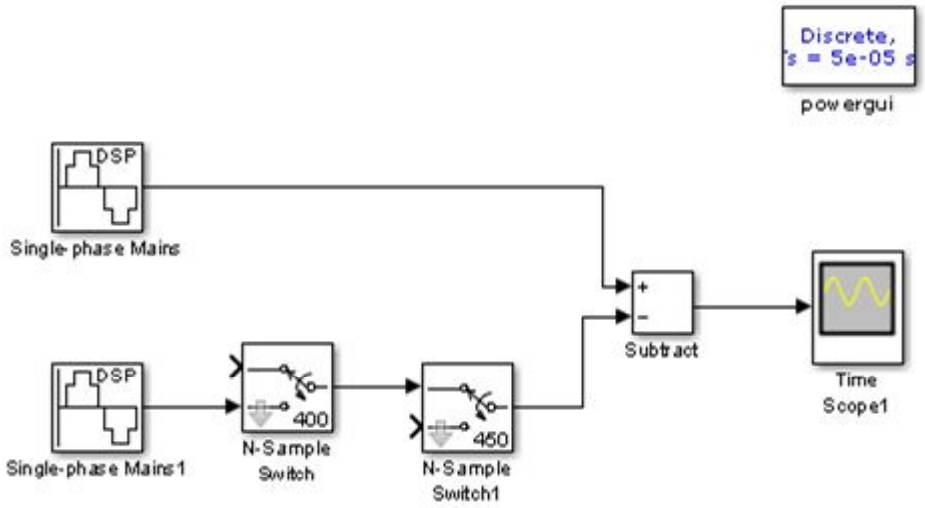

Figure 26 - Model to generate dips and swells in the input sinusoidal waveform.

Figure 27 shows the output for this circuit. The result was that the magnitude of the signal dropped during five half-cycles, starting at the beginning of a new cycle and ending in the middle of the third cycle just after the positive half-cycle terminated.

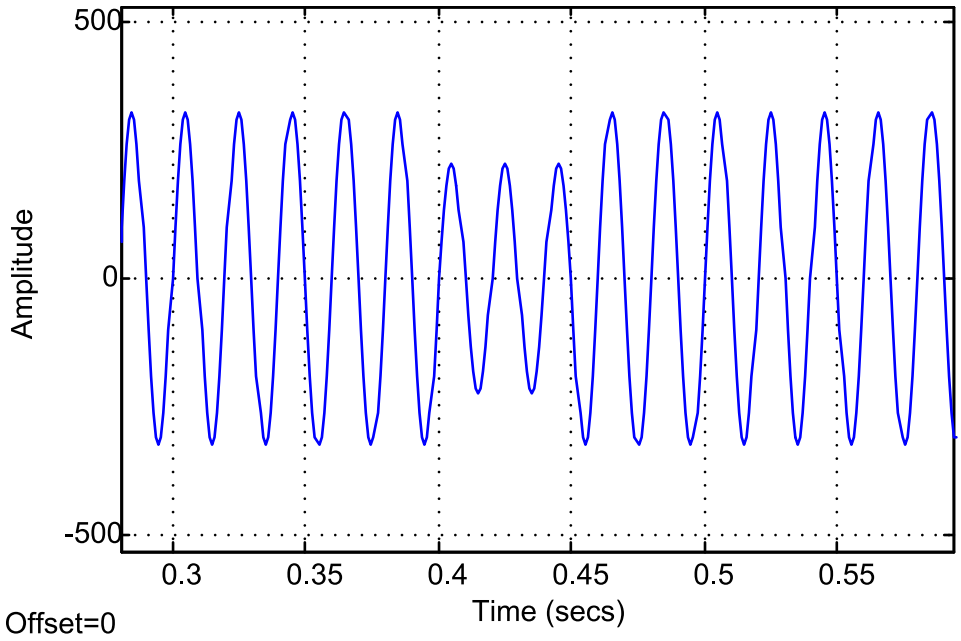

Figure 27 - A dip of 100V in magnitude 0.05s long.

For a swell where the wave magnitude had to increase instead of decrease, the same model could be used by replacing the subtraction operation with an addition operation. The wave would increase in magnitude during the period defined. The period was maintained the same as before in the model. The result can be seen in Figure 28. In this case the

magnitude increased from the beginning of a new cycle and returned to normal in the middle of the third cycle.

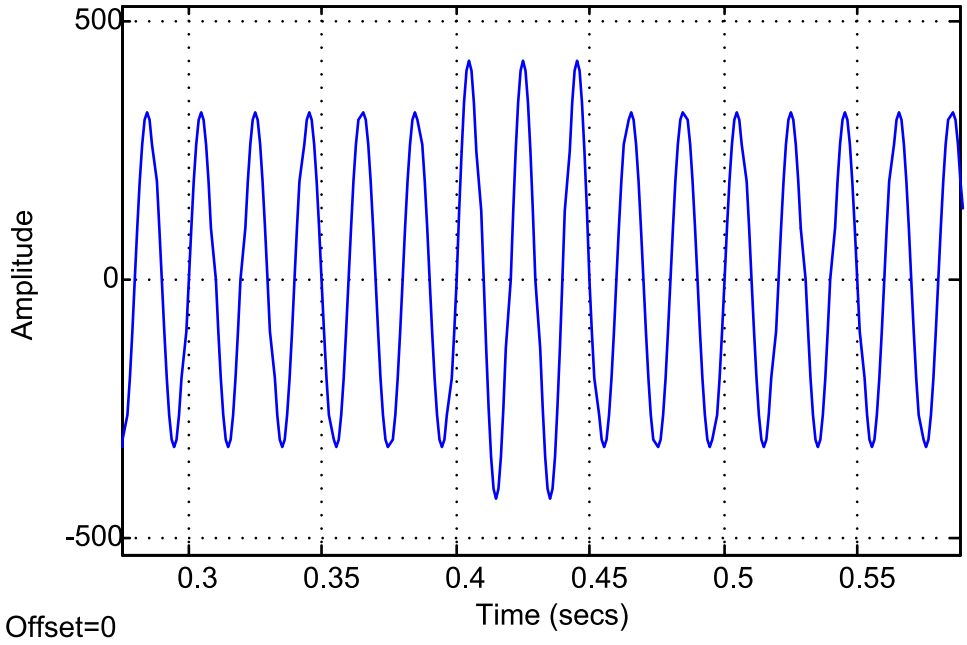

Figure 28 - A swell of 100V in magnitude 0.05s long.

Because a large dip (above 99%) can be classified as an interruption, it is possible to use the same model to generate this phenomenon. By subtracting the second wave with magnitude 99% of the first one or more, but below 100%, an interruption is generated. The result is shown in Figure 29.

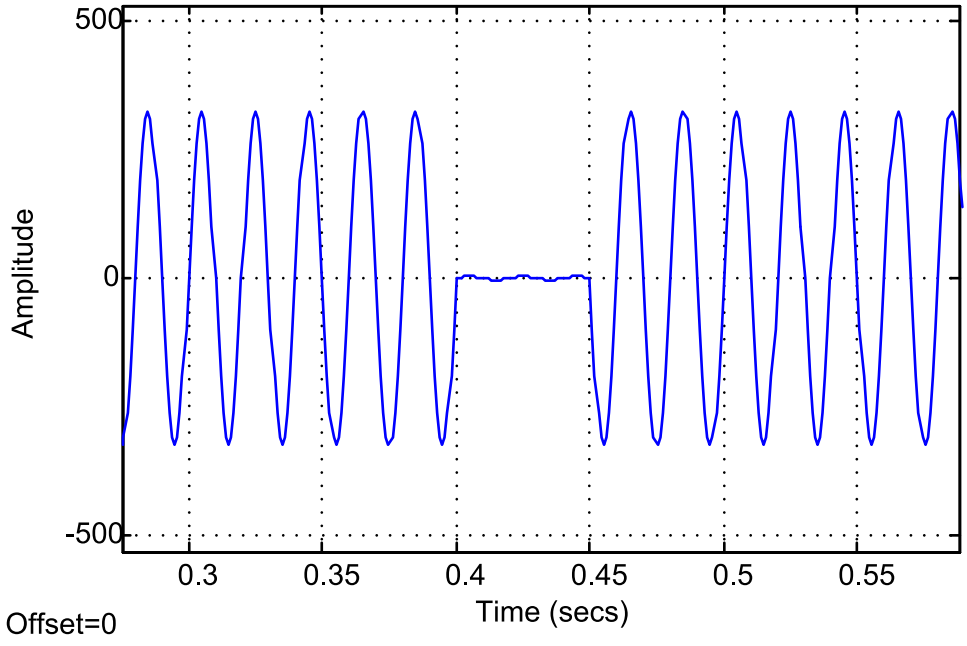

Figure 29 - An interruption 0.05s long.

4.1.3. A Model for Frequency Modulation

Although the expected frequency of the electric grid is 50Hz, this value may vary. To evaluate the monitor's capacity to measure these variations correctly, the model shown in Figure 30 was produced. It is basically a frequency modulator.

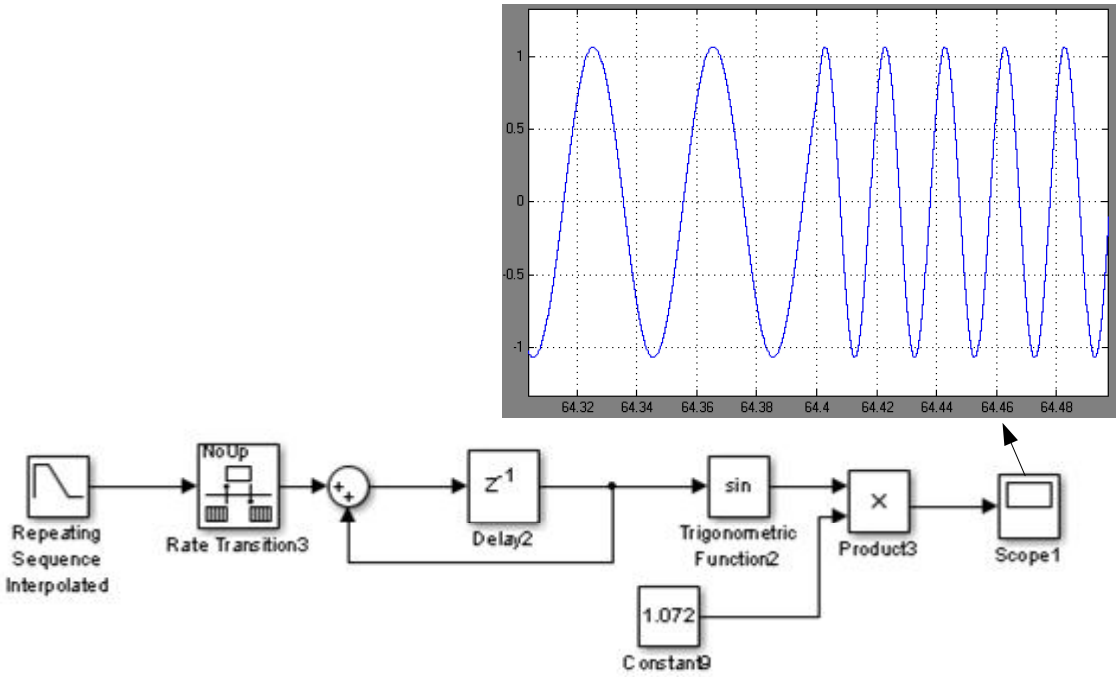

Figure 30 - Simulink circuit for frequency modulation.

The first block, repeating sequence interpolated, is used to define the equivalent angular rotation for a frequency of 50Hz followed by a new frequency rotation. The values will be set at the time instances set in the vector time values. Should the value for a frequency rotation be different at the next time instant, the value will alter linearly during the transition to reach the new value. The time instances can be moved closer together or further apart depending on the ramp size wanted. The frequency rotation can be either increased or decreased according to what is necessary. A rate transition block is used to interface the data rate so that it becomes compatible with the rest of the circuit. The adder and the delay form an integrator that will output a value incrementing linearly according to the value from the rate transition block. A trigonometric sine function is then used to reproduce a sine wave corresponding to each sample of the linear ramp at its input. The magnitude of the sine wave is then set by multiplying it with a constant factor. The value of 1.072 was used because the output waveform from the SOGI circuit is 1.072 also, intrinsic to the circuit constructed.

4.1.4. A Model for Harmonic Components

In a sinusoidal system like the electric grid, harmonic components are waves that are multiples of the fundamental wave's frequency, and appear superimposed on the fundamental wave. A large number of harmonics present deform the sine wave in such a way that it may become squarer in shape. Each of these components can vary in magnitude and affect the system differently.

To test the implemented circuit in detecting harmonics and measuring their magnitude, an adequate input signal model had to be implemented with Simulink blocks. To construct a composite signal with a fundamental frequency and the harmonic components expected to be detected by the measuring circuits, a discrete sine wave block should be used for each. Each one would be set with a different frequency starting at 50 Hz at the fundamental, while others would be set with higher multiple values thereof. The fundamental component, also known as the first harmonic, would be the predominant wave. Each of the blocks would have their magnitudes set. The values used were the ones indicated as maximum values in the European Standard. The blocks for harmonic components up to order 50 were combined with an adder block.

The magnitude values were introduced in a different way. Each harmonic component was set up with the respective frequency value with a magnitude set to one. Externally, a constant value could be multiplied with each harmonic component's output to reach the same result. A constant output would be expected from the model from start to finish.

The emergence of each harmonic component could be controlled the same way it was done with the simulations of dips and swells. Using two switches that could be configured to switch at specific samples allowed for this implementation as can be seen in the example in Figure 31.

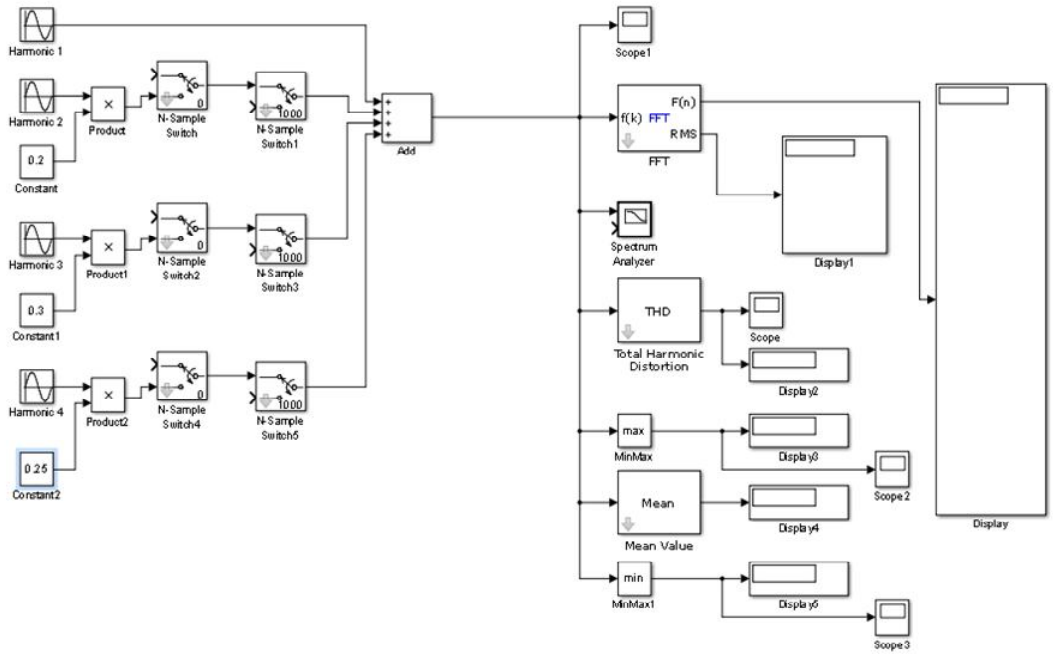

Figure 31 - Model for first 3 harmonic components.

4.1.5. A Model for Noise

Although noise is not a feature that has to be detected, it is easily present in any electric grid and measurement system. It is thus important to understand how the system reacts to it and therefore should be included in the testing of the implemented circuit. The fundamental wave was used for the base upon which the noise would be superimposed. This was done by using a random noise block with a variance set to 0.02 and the sampling frequency used for the sine generator block. To control the start of this noise and its duration, a discrete impulse was used with a delay of 49 samples and sample time of $75T_s$. Figure 32 shows this model and its respective output.

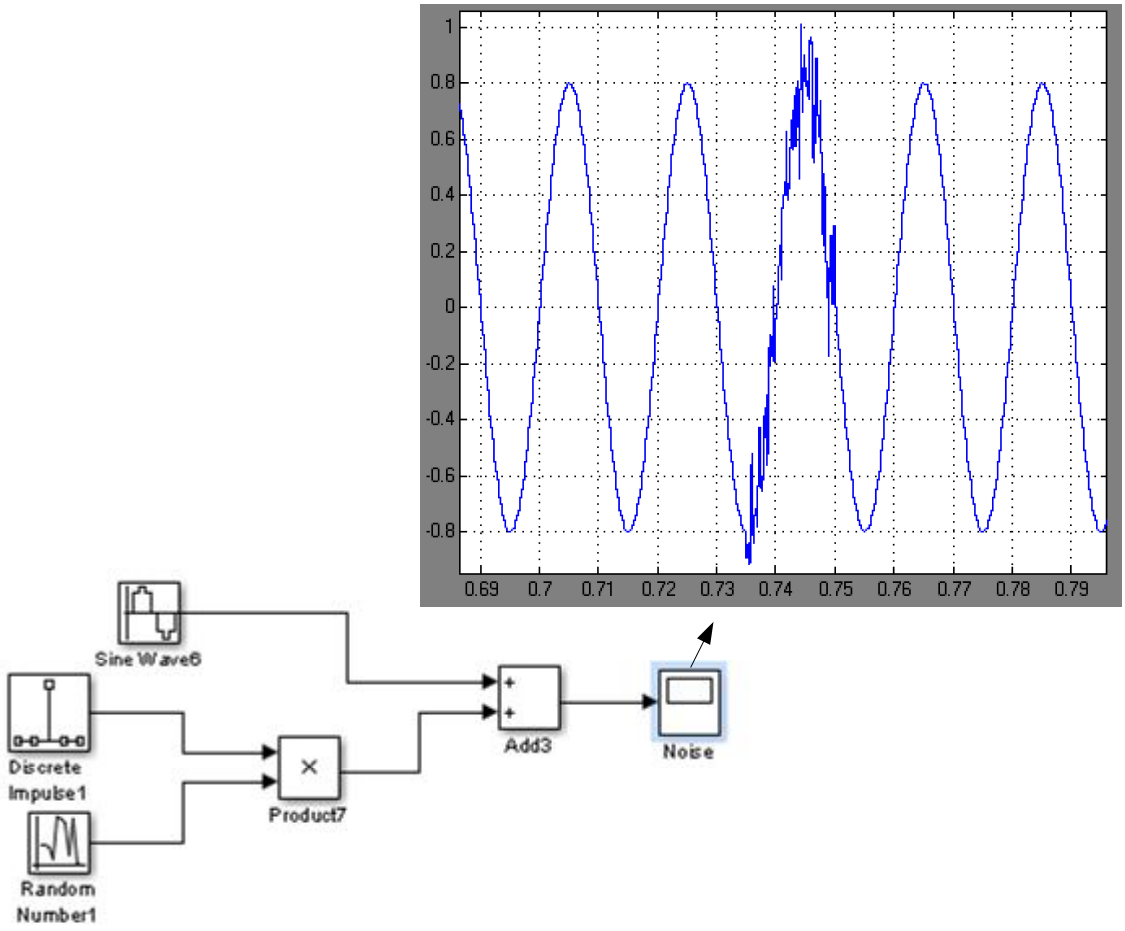

Figure 32 - The model for noise superimposed on the input signal.

4.1.6. A Model for Transients

A model such as the one used for frequency modulation was used to form the mainstream sine wave output as seen in Figure 33. This model has two branches: the first one generates the fundamental frequency waveform with a magnitude of 0.8; while the second one generates a sine wave of 1kHz and magnitude of 1. These two generated signals are added together at the end that results in the output shown in the scope output of the Figure.

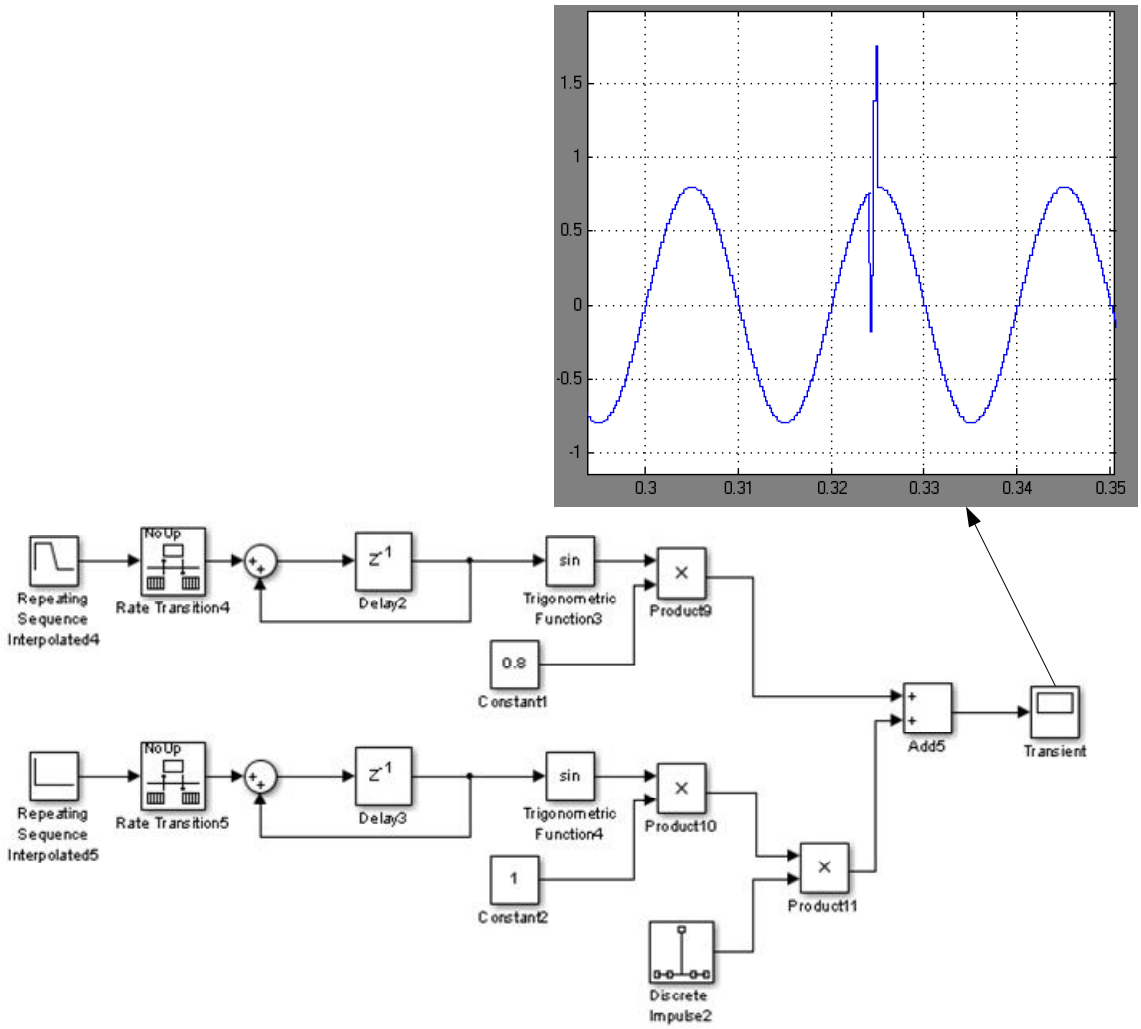

Figure 33 - The model for transients.

The repeating sequence interpolation block was used to define the frequency rotation necessary. A frequency change was allowed to occur as in real-life this can also happen. The rate transition block was then used to interface the data rate of the previous block to the remaining circuit. The values were integrated by the adder and the delay to obtain a linear ramp increasing in value. A sine wave was created from the input at the trigonometric sine function block that was then adjusted to the correct magnitude by multiplying its output with a constant factor of 0.8. Note that this is the expected nominal magnitude of the input sine wave.

Since transients are usually of much higher frequencies than the fundamental frequency, a second wave was generated to be added to the main one. A similar circuit as the one for the main waveform was used. The frequency rotation used in the repeating sequence interpolation had to be of higher value. The data rates had to be interfaced by the rate transition block as before then integrated by the adder and the delay. Creation of a sine wave was done by the sine trigonometric function block. A transient is usually of larger magnitude than the peak-to-peak value of the fundamental waveform so the constant by which the output was multiplied was one which was larger than 0.8. That output was then

made much shorter by filtering it with a discrete impulse before adding it to the base waveform. Various adjustments were made to obtain the final result where a transition appeared at the crest of a positive half-cycle.

Figure 34 shows a second version of this model where a repeating sequence interpolated block is used for the final filtering of the transient. Its purpose was to make the duration of the transient longer and to make it repeat when the sequence repeated.

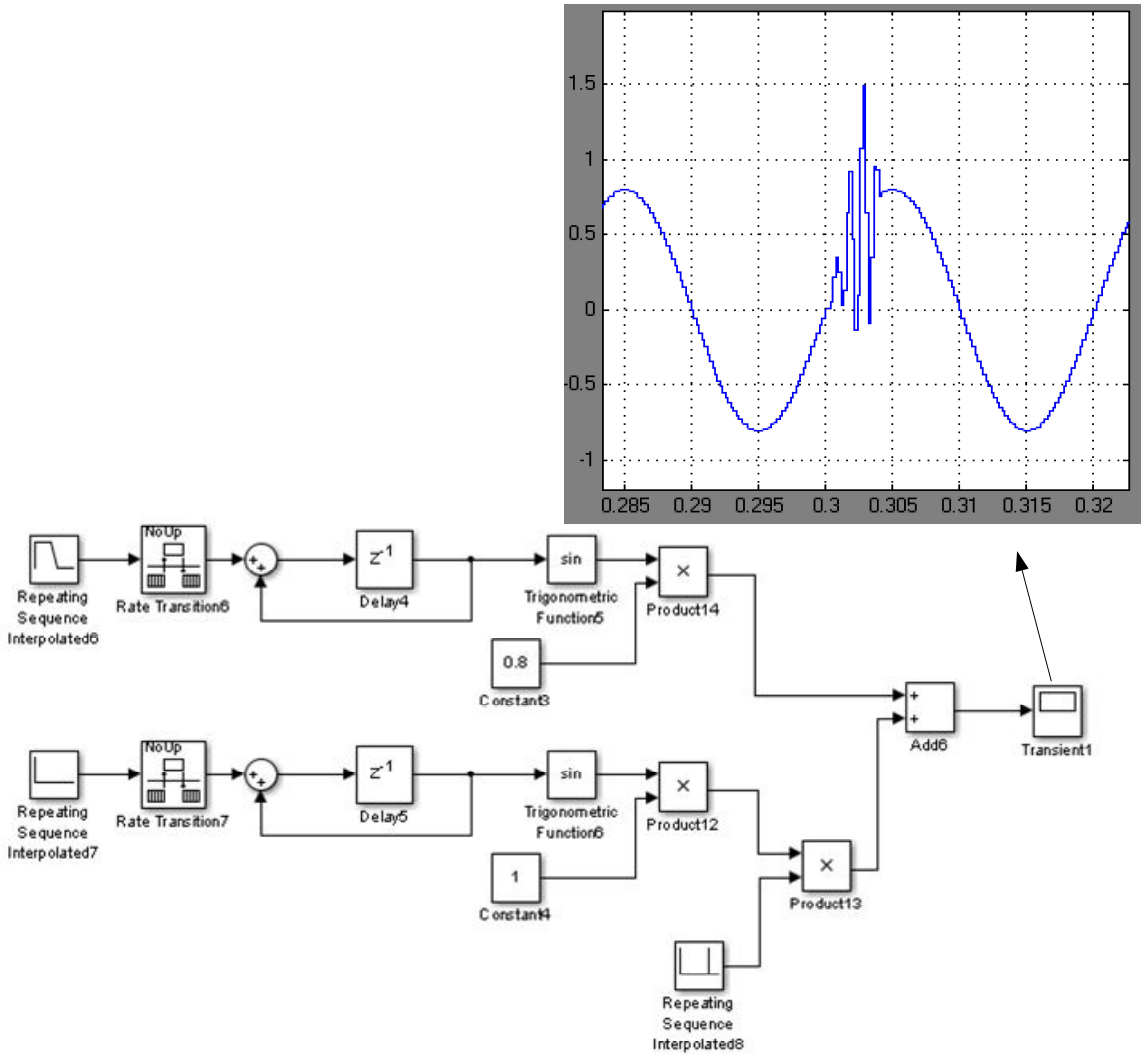

Figure 34 - A second model for transients.

4.2. Measuring Site Indices

Site indices, being the statistics of the aggregated characteristics of a site, are based on the parameters measured at that location. Experimental measurements were carried out by using the Simulink source models described in section 4.1. The processed outputs were fed to Simulink sink devices for visualization.

The basic sine wave model was used for the experiments to find out how accurate the measurements were. Various simulation runs were carried out for this. By altering the wave magnitude, peak values and rms values could be observed, as well as their resolution. From the very start of the simulation process, each cycle's peak value was measured. According to the fundamental frequency and magnitude subsystem's output, the maximum resolution of the fraction part of the value was 14 bits wide or 0.000061035 in decimal. A forced reset had to be implemented to reset the peak value measurement value or else it would only increment from the last value it had detected. This reset caused the positive peak value to reset to 0.0014 while the negative peak reset to – 0.0010. The difference in reset values is due to a difference of one sample period between their reset positions and completely negligible.

The rms value was only calculated at the end of each cycle so that all samples could be taken into account during the calculations. This method of post-processing is more than adequate because a result is obtained during the next cycle's positive half-cycle. The first value available in a simulation was always a very low value due to circuits not being completely stable from the very first sample. Since it would not affect aggregation values later on in the circuit, it was not removed. A second value was already very close to the value expected although not yet correct. The value available after the third cycle being complete would be the expected result.

Table 9 shows some of the results obtained from a few simulations after ensuring that the calculations were correct. It can be seen that overall the values are acceptable due to the negligible difference between expected and measured values not exceeding 0.0001 which is equivalent to 0.014142 on the 0 to 230 scale.

Table 9 - Comparison between expected and measured rms values.

		V				
	Input	0.8	0.799652	0.793043	0.799130	0.798991
rms	Expected	0.32	0.31972	0.31445	0.31930	0.31919
	Measured	0.3199	0.3197	0.3144	0.3193	0.3192

For the fundamental frequency tests, the frequency was altered up to the third comma place. The results can be seen in Table 10. From the number of samples used for capturing each cycle, a 50Hz wave would be broken up into 16.384 time frames. Each of these time frames represents 0.00305175Hz, as long as enough bits are used in the frequency measurement unit.

Table 10 - Comparison between expected & measured fundamental.

		Hz				
	Input	50	49.99	49.985	49.983	49.984
Fundamental Frequency	Expected	50.00	49.99	49.985	49.983	49.984
	Measured	50	49.9908	49.9847	49.9817	49.9847

All samples had to be collected before the calculations could be made; therefore a post-processing calculation for the value was done. This value was available shortly after the end of the cycle being analysed. The value for the first cycle was always extremely high due to an extremely low sample count available at the time to be used. A circuit was implemented to maintain the divide block reset during the first two cycles although the counter was allowed to accumulate the number of samples during the second cycle. This safety would keep the divide block from calculating the erroneous value. The calculation being done after the completion of the cycle made it possible to have the first acceptable value at the end of the second cycle. Although the value was close to the expected value, it was not entirely correct. The effect of this value during the aggregation periods would be negligible. From the third cycle the value was correct.

The time aggregations that were implemented were verified. Each timer was run completely autonomously from each other. As each measurement was made by the fundamental frequency and magnitude subsystem, these output values would be accumulated when the data became available and indicated by the data valid. The totals were then divided by the number of accumulated values in each case, when the timer reached the end. The aggregation periods were connected in a cascade configuration so that the first aggregation was available to the next one for accumulation. For example, five values from the 200 ms aggregation were used to calculate the 1 s value, and so on. The testing revealed that these circuits functioned correctly.

Due to the use of a lighter version for the testing, the zero-crossings have a large error, the size of T_s, in the estimated crossing through zero. It is necessary to take this into account when analysing the results.

Tests were also carried out with white noise superimposed on the input signal. The filter did its work, as expected, adding to the quality of the measurements. Harmonics 2 and 3 were both present during these tests with magnitudes as indicated in the European Standard EN50160 at their maximum acceptable levels.

Tests to verify the system’s reaction to fast magnitude changes were carried out. Figure 35 shows the value with which the input was multiplied to force these fluctuations. From 0 to 0.4s the input remained at the nominal expected value then dropped to 40% of that value until 0.6s, returning back to normal until 0.8s. Between 0.8s and 1s it increased to 120% then dropped below the nominal value to 90% until 1.2s.

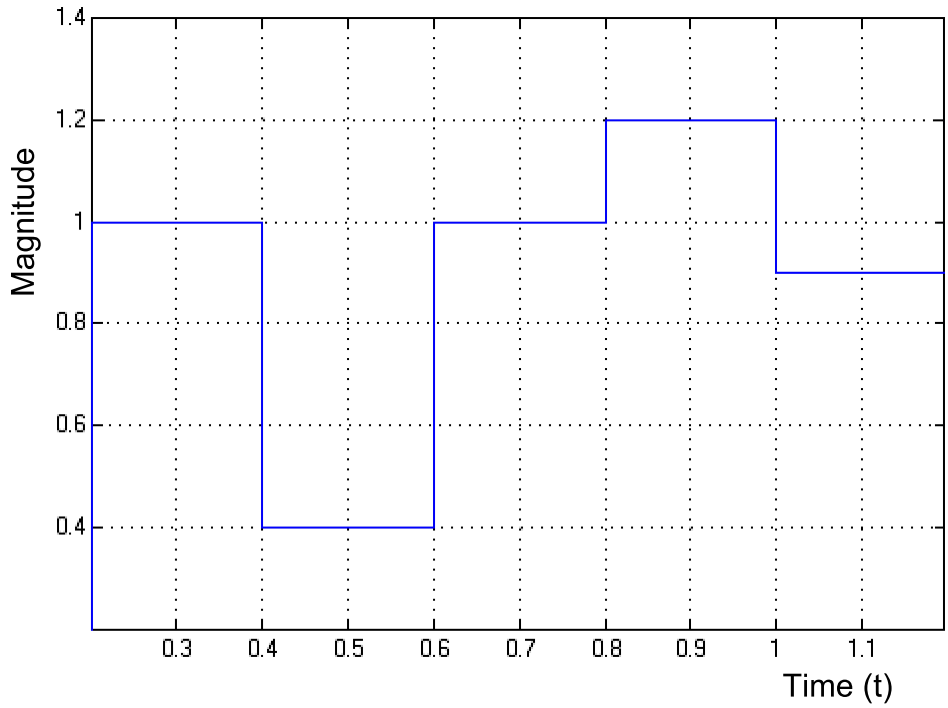

Figure 35 - Sudden step changes multiplied with the input waveform.

Figure 36 shows part of the graph from Annex 9 with an input sine wave and sudden changes in magnitude. Positive and negative peak value measurements and the calculated rms value (still to be square-rooted) are shown. The results were obtained from the system using 6400 samples per cycle.

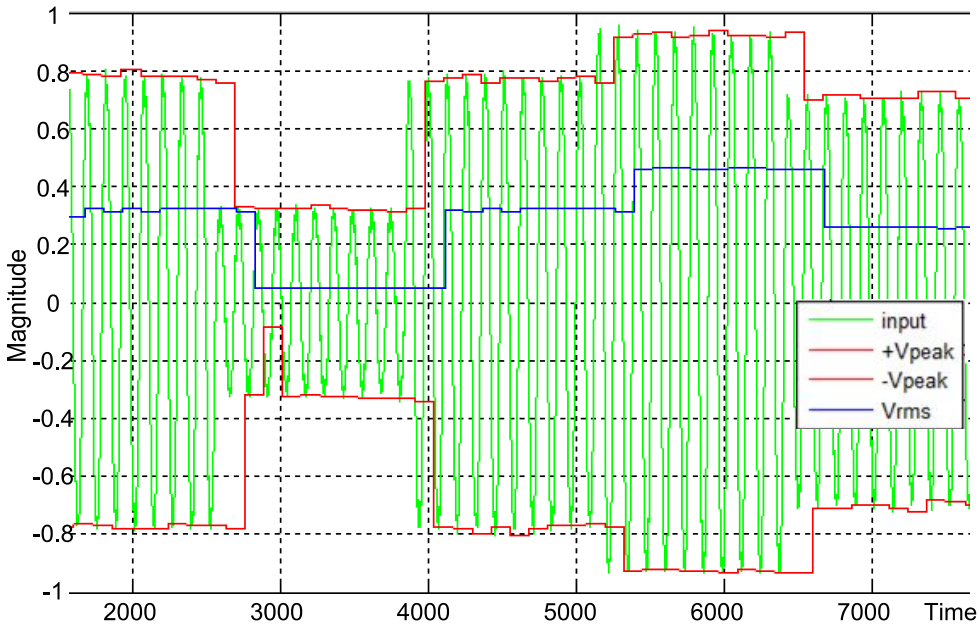

Figure 36 - Unfiltered measurement of magnitude variation with noise.

Both the positive and negative peak values follow the input value closely with a short delay. The values measured are not stable as noise was also injected into the input signal

and these measurements were done without the use of a filter. The rms value showed a slightly larger delay in response to the input values and show more stable values. The input repeated again continuously after this window of measurements.

The same tests were done on the system after filtering, shown in Figure 37 as part of Annex 10. Again the input waveform is shown with the positive and negative peak value measurements. The rms value is also shown.

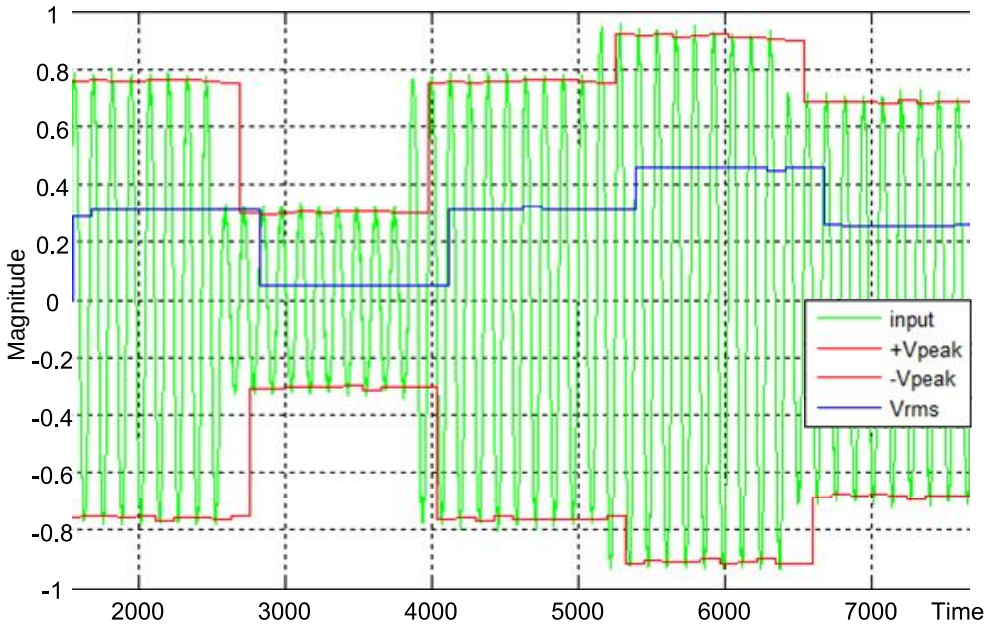

Figure 37 - Filtered measurement of magnitude variation with noise.

The measured value deviations were lower in comparison to the unfiltered system's measurements. The output values in the graph are more flat in nature with the use of the filter. The rms values were also steadier than in the previous system. This window of measurements was in continuous repetition.

The same tests were carried out with a level of 10% noise on the system without filtering. The results are available in Annex 12. Figure 38 shows the summarized version of these results. The noise level was very high, beyond what can be expected on a day-to-day basis in the electric grid, which resulted in problems with the zero-detecting circuit unit. This is the reason why the results are so bad.

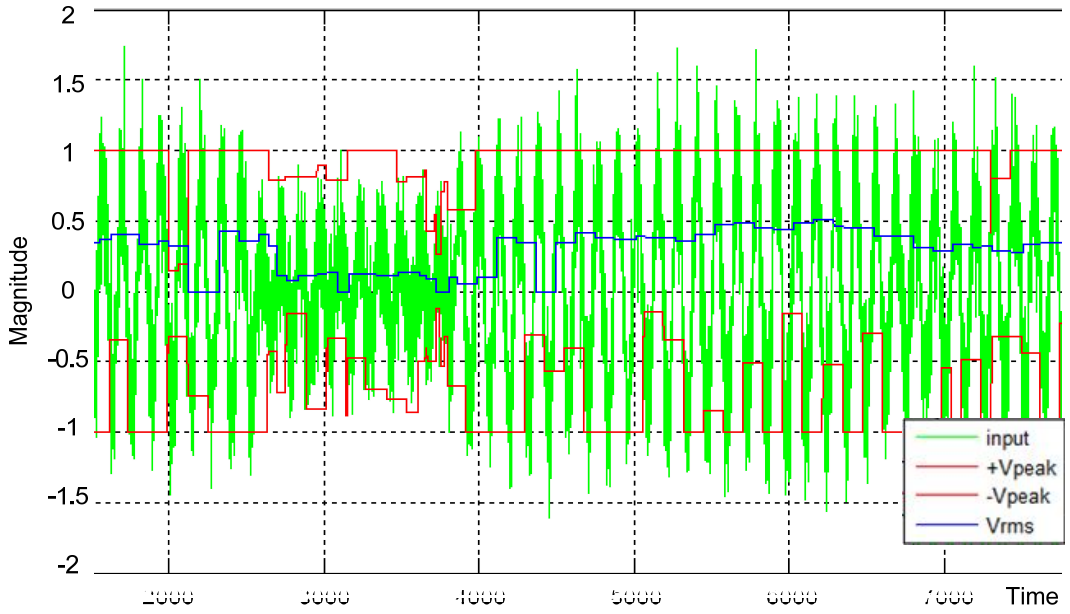

Figure 38 - Unfiltered measurement of magnitude variation with 10% noise.

A very heavy noise component was superimposed on the input. Even so, the unfiltered measurements were made although some values are unrealistic as they do not go beyond the value of one. The calculated rms values are more realistic. These tests were also carried out on the filtered system as shown in Figure 39.

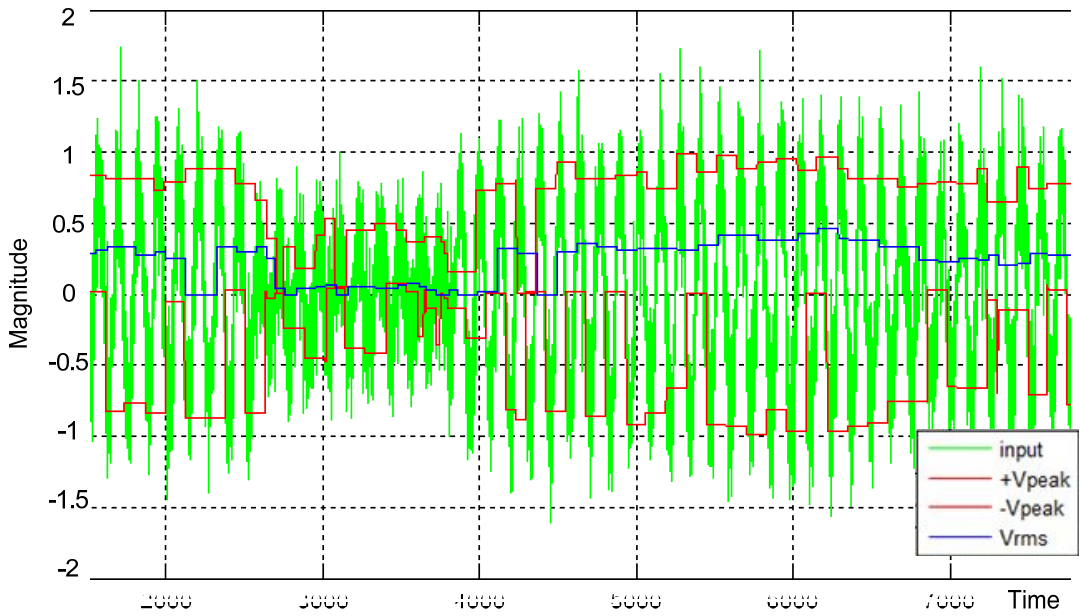

Figure 39 - Filtered measurement of magnitude variation with 10% noise.

These positive peak values are more realistic together with the calculated rms values. The negative peak values have large fluctuations. These measurements with 10% noise are beyond the limits of the system.

4.3. Measuring Harmonic Components

The harmonic components, multiples of the fundamental frequency, up to order 50 could be measured and the inter-harmonic components, non-multiples of the fundamental frequency, in-between too. Various trials were carried out with outputs to the power spectral analyser in Simulink. Although the results with higher resolution would have been better, due to the simulation being too long, the results were obtained with a lighter version using a lower amount of samples. Some tests were done with full resolution.

Figure 40 shows the FFT output for the fundamental frequency of 50Hz with a magnitude of 1.

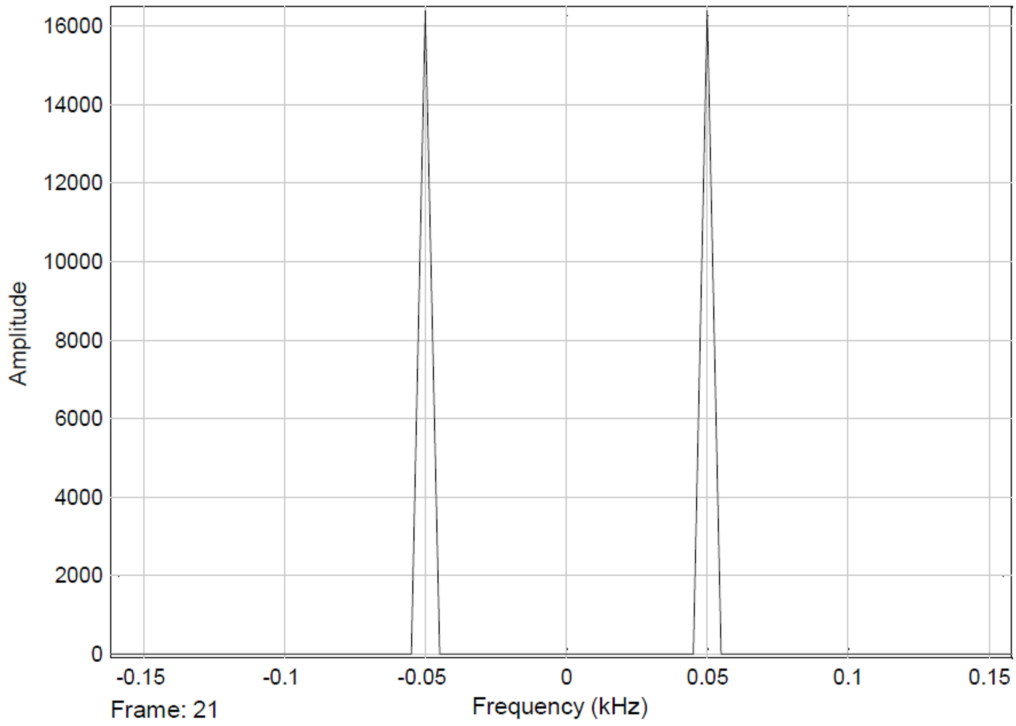

Figure 40 - FFT output of 50Hz fundamental frequency.

The measurement result is exactly at 50Hz with a magnitude of 16384 which represents a true magnitude of one. No harmonic or inter-harmonic content was present. Figure 41, on the other hand includes harmonic 2 and harmonic 3.

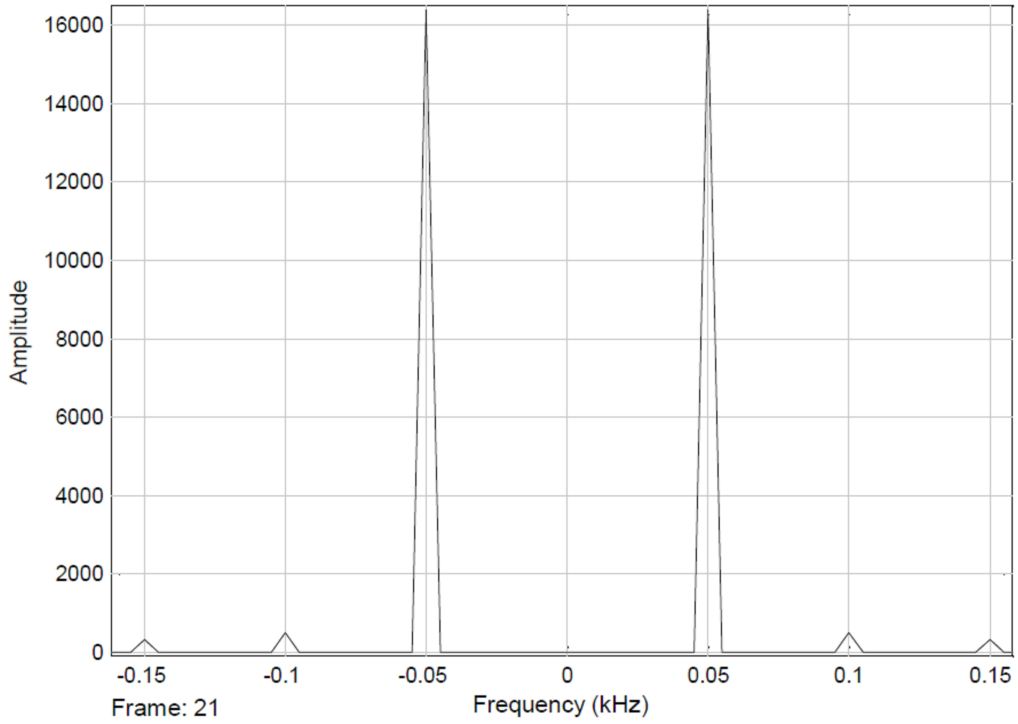

Figure 41 - FFT output with fundamental, harmonic 2 and harmonic 3.

Harmonic 2 had a magnitude of 3% and harmonic 3 had a magnitude of 2%, values referenced to the nominal magnitude of one. Each measurement corresponded to the correct frequency bin. Figure 42 shows a different fundamental frequency of 37.5Hz with harmonic 2 and harmonic 3 being multiples of its frequency.

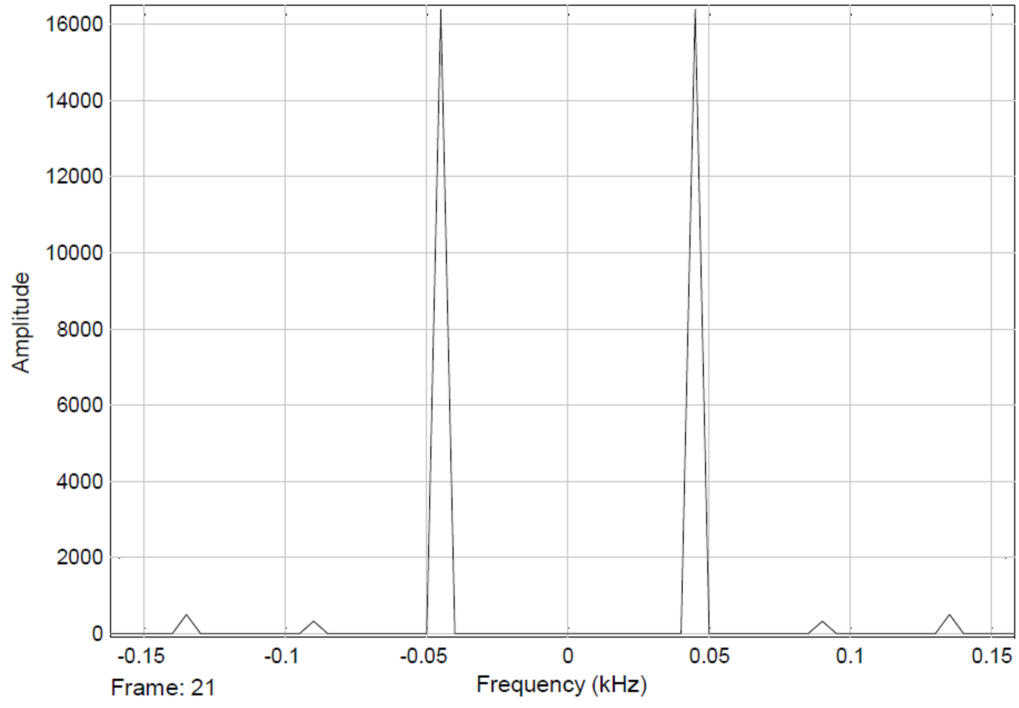

Figure 42 - FFT output of 37.5Hz fundamental and its first 2 harmonics.

Here the harmonic component magnitude for harmonic 2 and 3 were altered to be 2% and 3% of the nominal value respectively. As can be seen, the frequency bins were different to the ones before as expected coinciding with the respective frequencies.

Tests were then carried out and both results from the Simulink power spectral analyser as well as the System Generator power spectral analyser were gathered. Figure 43 shows the spectral measurement with 12.5Hz frequency bins.

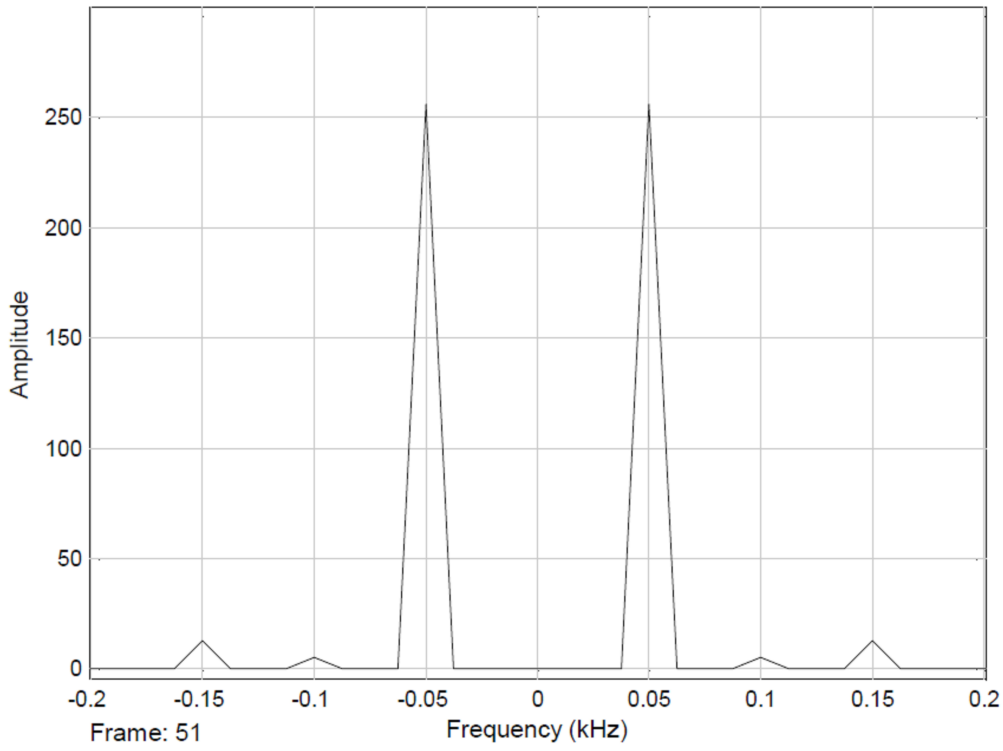

Figure 43 - FFT output with bins of 12.5Hz.

The tests were carried out with fewer samples at the input which resulted in a lower magnitude of the fundamental frequency compared to the values before, although still representing the magnitude of one just the same. Harmonic 2 was at 2% and harmonic 3 at 3% of the nominal value of the fundamental frequency. Figure 44 shows the results obtained from the System Generator power spectral analyser.

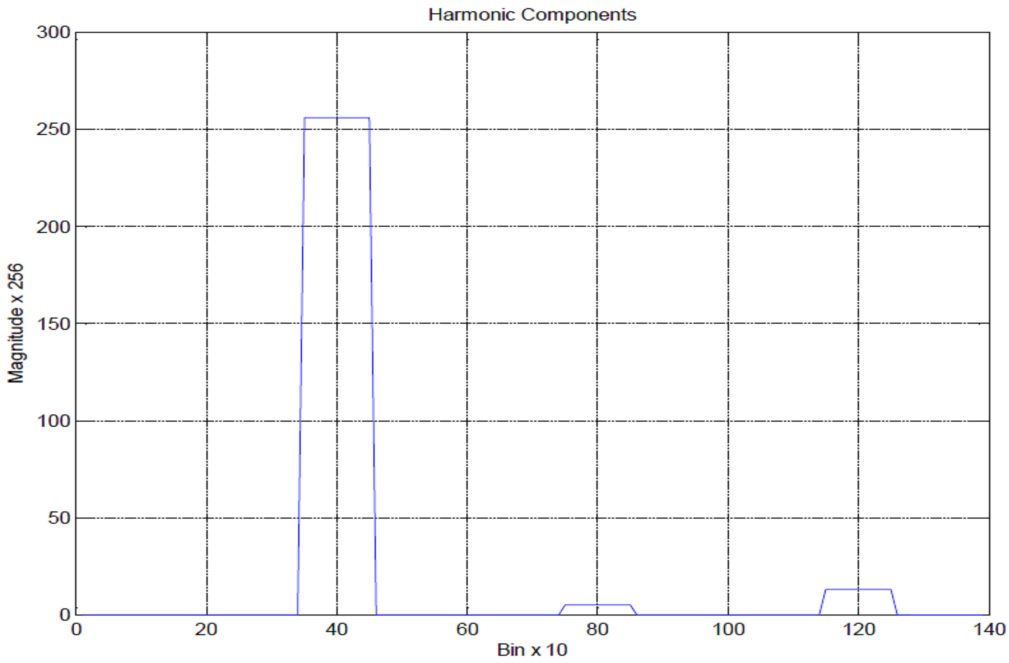

Figure 44 - Respective frequency bins and magnitude measured.

The values measured by the System Generator power spectral analyser were plotted in a graph for better perception of the results. The fundamental frequency corresponded to bin number 4, harmonic 2 to bin number 8 and harmonic 3 to bin number 12. The magnitude values measured were correct. A similar test was done with a different fundamental frequency value as shown in Figure 45.

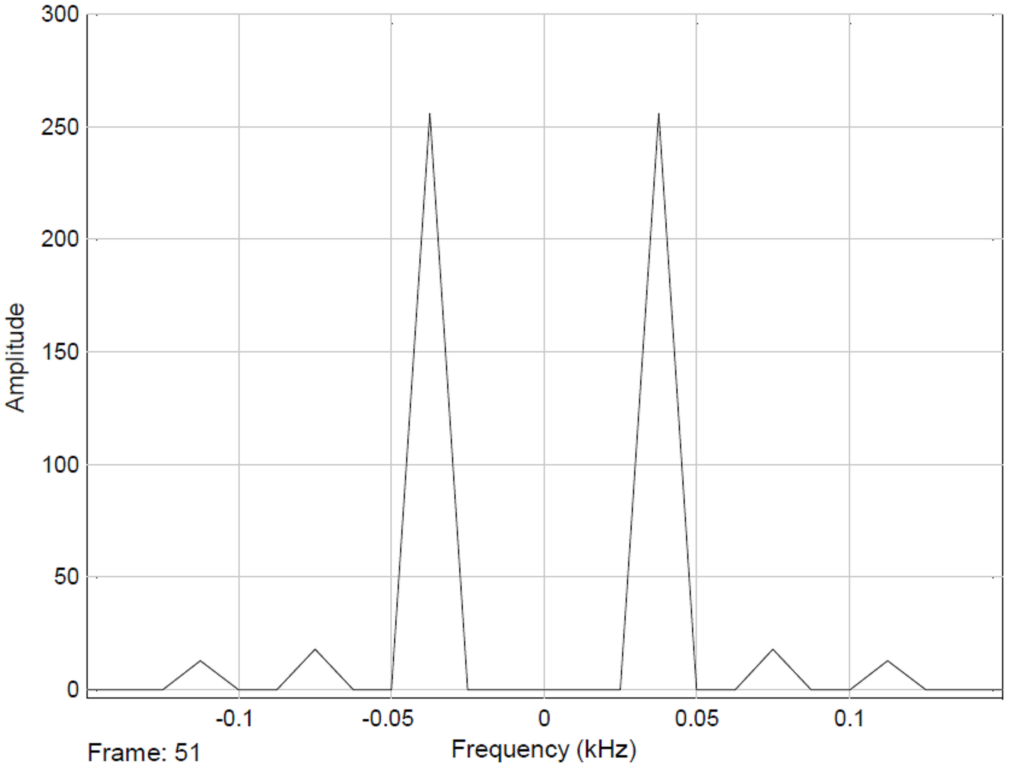

Figure 45 - FFT output for a fundamental of 37.5Hz and bins of 12.5Hz.

Harmonic 2 had a magnitude of 3% while harmonic 3 had a magnitude of 2% and corresponded to the 75Hz and 112.5Hz frequency bins respectively. Figure 46 shows the System Generator power spectral analyser measurements.

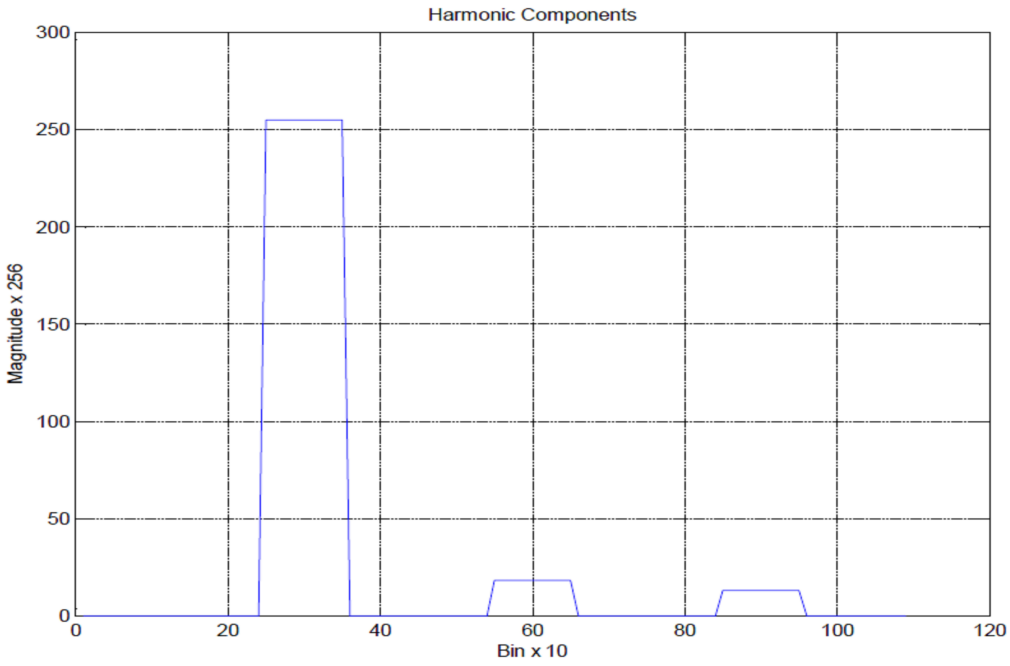

Figure 46 - Measurements for 37.5Hz fundamental and its 2 harmonics.

The fundamental frequency bin was number 3. Harmonic 2 coincided with bin number 6 while harmonic 3 was detected in bin 9. Their magnitudes proved to be correct. A zoomed version of Annex 15 can be seen in Figure 47 of the full spectrum with fundamental frequency at 50Hz and the first 25 harmonic components. The frequency bin size is 10Hz wide.

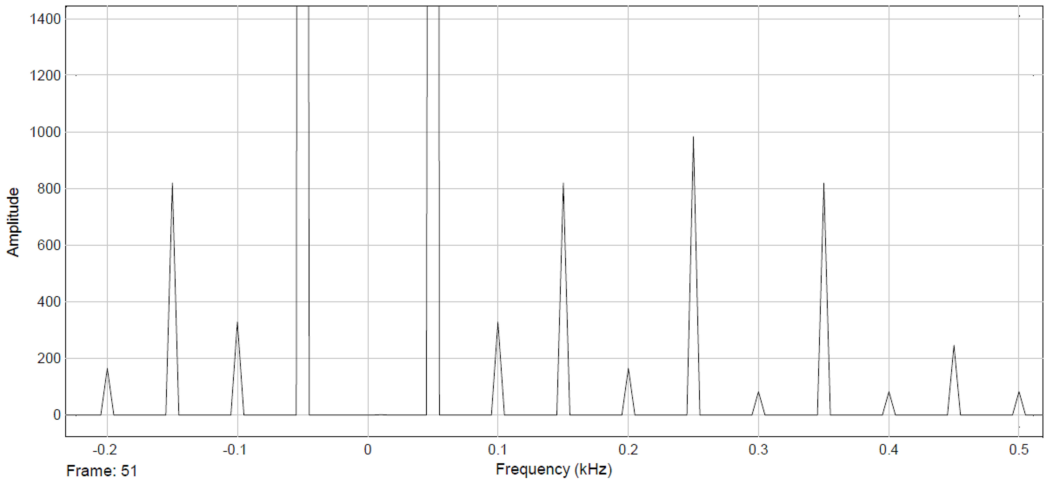

Figure 47 - The zoomed version of harmonic 1 and the next 9 harmonics.

The Figure shows the fundamental frequency at 50Hz and harmonic 2 to 10. The magnitude values are considered by the European Standard to be the limit. The magnitudes appearing between these frequency bins would be the inter-harmonic frequency signals.

Annex 11 and Annex 14 show plotted values for the system with the presence of noise and noise at 10% respectively. They show the input signal, the measured fundamental frequency, the fundamental wave's magnitude and the fundamental frequency bin. The tests were done with a very low amount of samples. Annex 16 shows the full spectrum with 25 harmonic components with frequency bin size of 1.5Hz. Annex 17 shows an unexpected spectrum with a fundamental frequency of 50Hz and inter-harmonic components at frequencies 147Hz, 148.5Hz, 151.5Hz and 153Hz.

4.4. Measuring Events

Events as opposed to stationary signals are considered as fast deviations from the expected wave of the electric grid. These phenomena are best detected by comparing the input against the ideal wave generated internally by the monitor. The advantage of using the Phase-Locked Loop circuit is that it generates a waveform that tends to follow the input with equal frequency and magnitude without sudden deviations. The difference between the input wave and the PLL generated wave will result in the event detected.

The PLL system time response was evaluated by running a set of initial tests. The results are shown in Table 11.

Table 11 - System time response due to FIR stop frequency.

	Time response (s)	
Phase angle θ	FIR 50 Hz	FIR 100 Hz
0	0.4446	0.2350
¼ π	0.4021	0.2025
½ π	0.3897	0.1800
¾ π	0.2871	0.1077
π	0.3447	0.1550
1 ¼ π	0.3521	0.1626
1 ½ π	0.3696	0.1700
1 ¾ π	0.3971	0.1976
2 π	0.4446	0.2350

The tests were carried out for two different stop frequencies adjusted on the FIR filter for various combinations of input signal phase variation. The synchronization was faster for a stop frequency of 100Hz on the FIR filter and in both cases a phase lock was fastest when the input had a phase shift of $\frac{3}{4}\pi$. This is also seen from the plot in Figure 48.

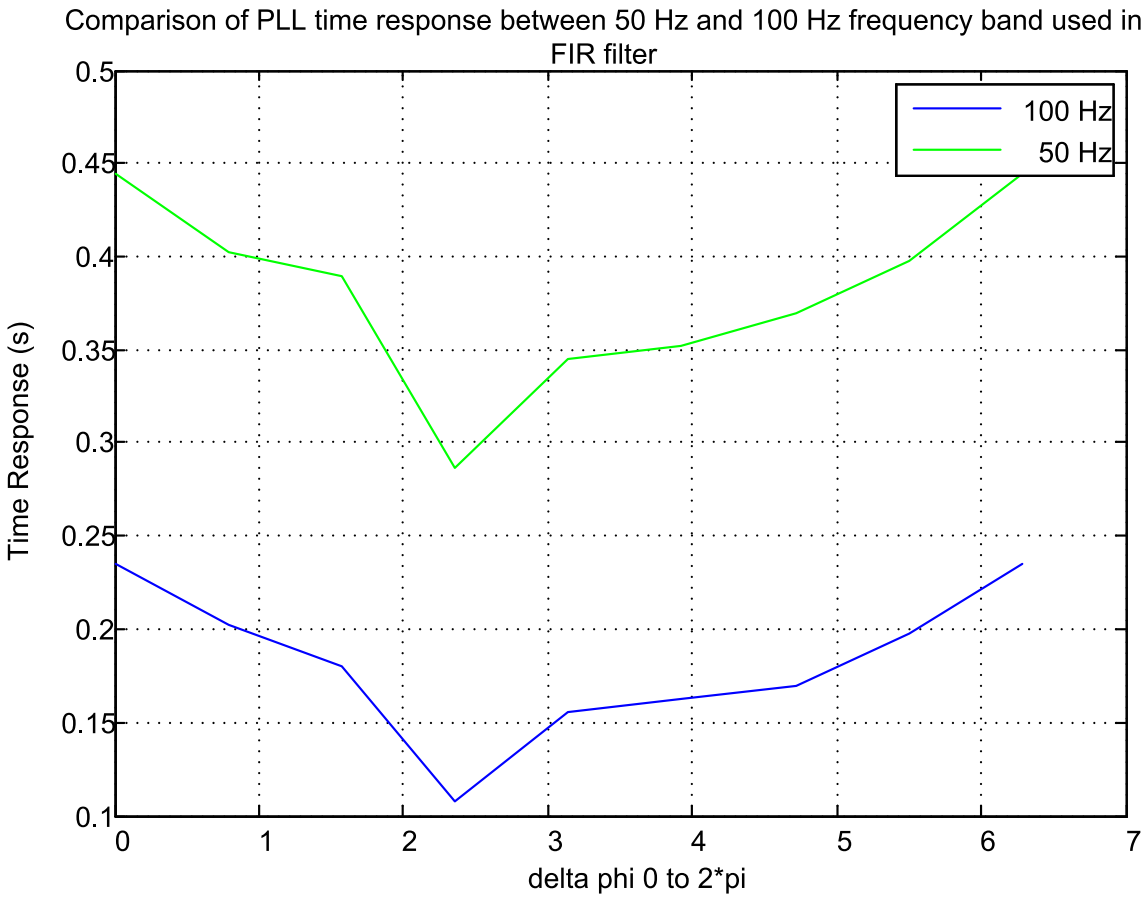

Figure 48 - Time response comparison between two FIR filter parameter values.

After circuit stabilization, the mean μ and the variance σ^2 were found for the FIR filter output and the PLL output as shown in Table 12.

Table 12 - Mean & variance of FIR filter & difference between input & PLL.

	mean μ	variance σ^2
FIR output	-2.40786e-06	2.11668e-08
Error between input & PLL	0.000464	0.037296

The PLL circuit on start-up takes a few cycles to follow the input signal correctly so ten cycles were considered for this stabilization. The circuit is unable to follow sudden alterations. This characteristic of not being able to react quickly to a change makes it useful to use it as a reference signal.

The system's time response was also tested with three frequency steps that were placed at the system input: the first with transition time t = 0 s in Figure 49; the second with transition time t = 0.2s in Figure 50; and the third with transition time t = 0.6s in Figure 51.

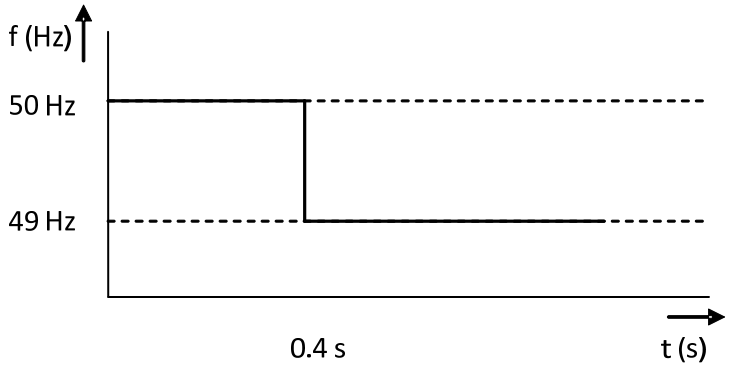

Figure 49 - An input with frequency step of x = 0 seconds.

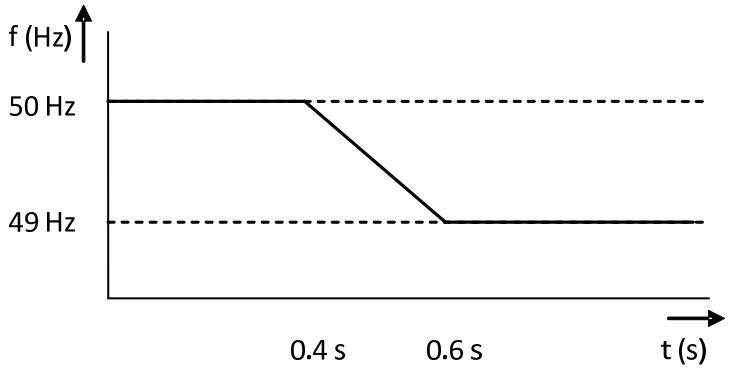

Figure 50 - An input with frequency step of x = 0.2 seconds.

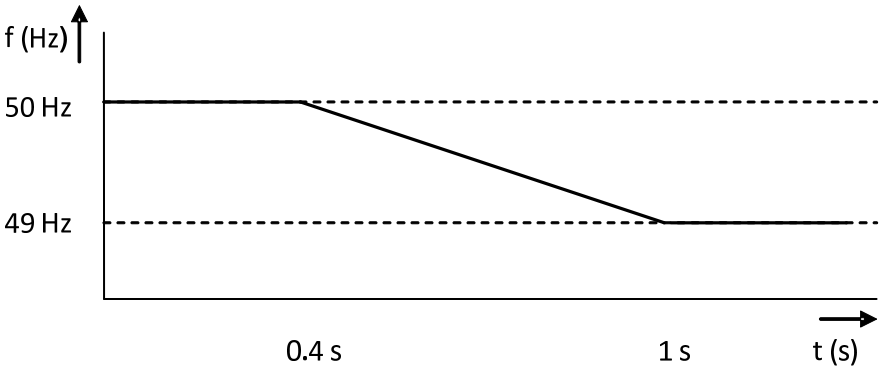

Figure 51 - An input with frequency step of x = 0.6 seconds.

The results are shown in Table 13. The time response was three and a half cycles for a step with zero transition time while the others were longer. Annex 20 shows the FIR filter output adjusting gradually to the input, it also shows how the PLL output follows the input (top graph in green with higher magnitude).

Table 13 - Time response for each step input.

Step (s)	Time response (s)
0	0.07
0.2	0.235
0.6	0.6

The normal in-phase / quadrature output was a sine wave and cosine counterpart, both of magnitude 1.072. To use this wave as the reference wave against which the input of magnitude 0.8 would be compared, a compensating circuit had to be used. The output magnitude of the PLL was measured with the fundamental frequency and magnitude circuit. The PLL magnitude was then divided by the measurement made to normalise the value after which it was multiplied by 0.8. Finally the difference between the input signal and the generated PLL signal can be made available to the processor for statistic and post processing.

Various groups of tests were carried out to verify the performance of the event detecting circuitry. A variety of dips, swells, an interruption, noise and transients were simulated and each programmed to launch after the PLL had settled down. These were divided into two sections: a) dips; b) swells and other events.

4.4.1. Dips

Regarding dips, the criteria of the European Standard EN50160 was used as the basis for the simulation, as shown in Table 14.

Table 14 - Dips chosen for simulation according to EN50160.

Residual voltage u	Duration t (ms)				
(%)	$10 \leq t \leq 200$	$200 < t \leq 500$	$500 < t \leq 1000$	$1000 < t \leq 5000$	$5000 < t \leq 60000$
$90 > u \geq 80$	1 & 2				7
$80 > u \geq 70$		3		8	
$70 > u \geq 40$			4		
$40 > u \geq 5$		9		5	
$5 > u$	10				6

The table allows for a variety of different situations, from shallow dips of short duration to very deep ones of very long duration and all those in-between. This table shows the dips that were selected by their number for the simulations as these were considered to be the more representative cases. They were chosen for being the diagonal cases that included the extreme situations. Each number in the table represents a different simulation.

Dip 1, chosen to have a short duration of 10ms and to cause a drop in magnitude from 100% to 82% was launched at around sample 1225. This is reflected in Figure 52. This Figure is composed of three graphs: a) input signal to be measured; b) the positive peak and the half wave rms values that are measured by the measurement unit; c) the error between the input signal and the internal generated PLL waveform, in other words the event. The input waveform was normal until around sample 1225 where the event occurred. Since the event was only one half-cycle long, the decision was made to have it appear so that it would be distributed equally between positive and negative half-cycles.

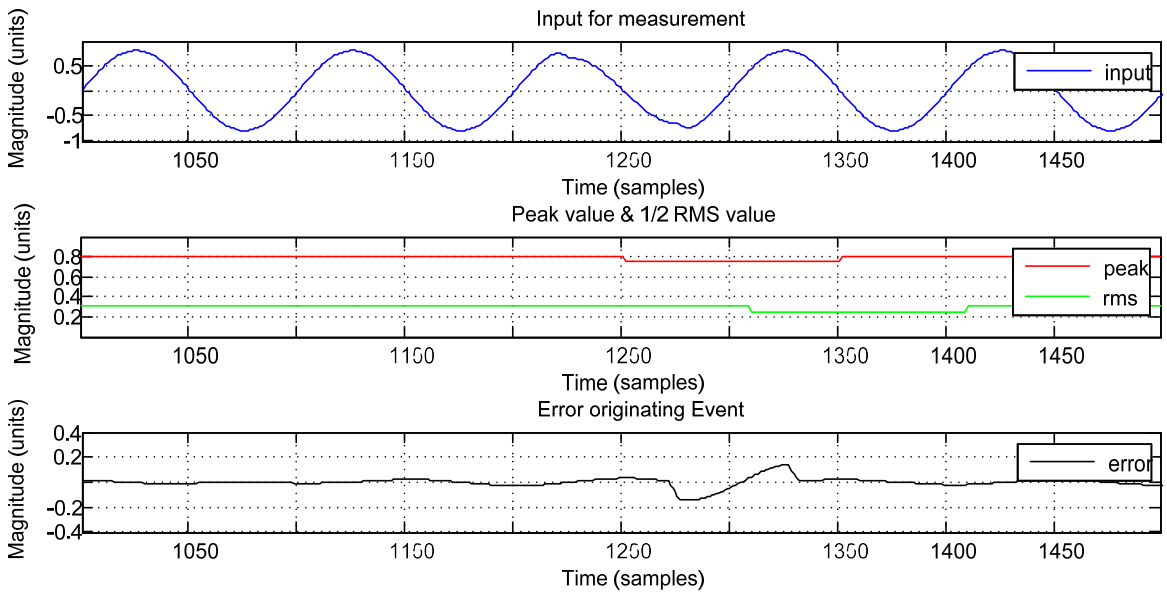

Figure 52 - Results for the detection of dip 1.

The event detection circuit detected the lowering of the positive peak value, also captured by the Vpeak measurement unit. The delay between the dip's initiating instant to the peak value reflecting this change was due to circuitry delay. Negative peak values are not shown to prevent crowding of information in the image, although this value was also measured.

The rms value for each half-cycle reflected the detection by the lowering of the value from the previous cycle respectively, represented in green. Due to more complex circuitry in calculating this half-cycle rms value, a larger delay can be seen from the point where the dip was launched until the result was reached. The full-wave rms value, although measured by the circuit, was not shown due to it not adding any fundamental value to the discussion.

The curve in black, which is the error between the input signal and the one generated by the PLL, allows the system to detect the dip and its duration. This error signal allows the system to identify that a disturbance is occurring and returns to zero as soon as it ends. The small increase in error is an indication that a relatively small difference in magnitude between the two waves occurred.

Dip 2, two and a half times longer than dip 1, and also dropping the magnitude to 82%, was launched at the same time instant as the one before. Figure 53 shows this dip that was just over one cycle long.

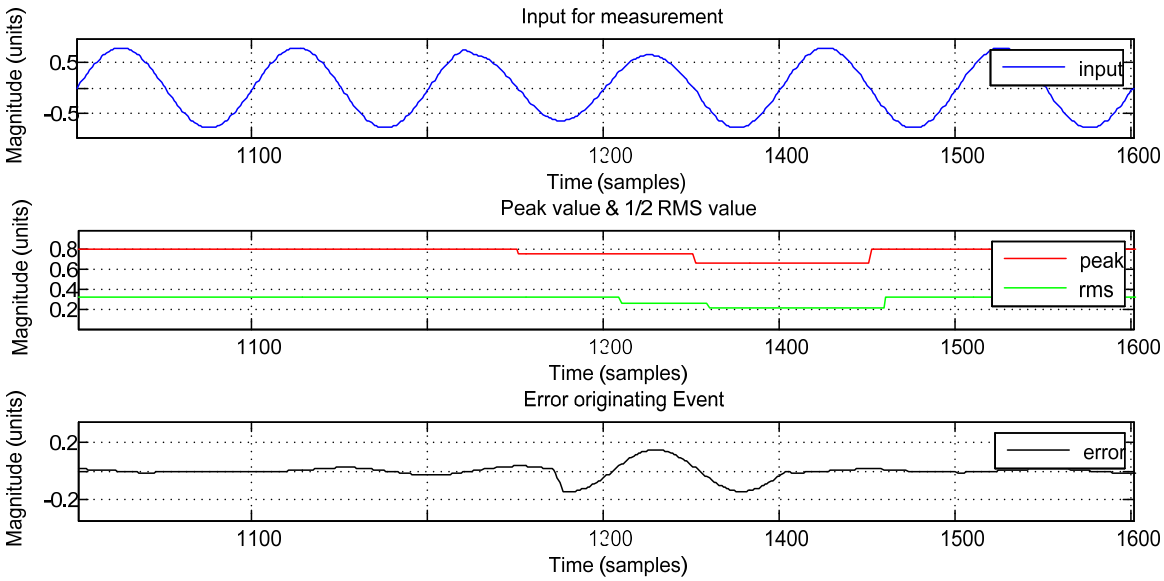

Figure 53 - Results for the detection of dip 2.

The positive peak value dropped twice in two equally long steps. This was due to the dip having only partially affected the positive half-cycle in which it started, and having affected the next half-cycle completely. The full depth of the dip was identified in the negative peak value between these two half-cycles. The half-wave rms value indicated this with the second step being twice as long as the first. The error between input wave and the PLL generated wave was of the same magnitude but of longer duration.

Both dip 1 and dip 2 would be classified per the European Standard as being of the same type since they are both within 10ms and 200ms time duration and within 80% to 90% magnitude from the nominal value.

Dip 3 was simulated for a period of 210ms to drop the magnitude to 74%, shown in Figure 54. This dip would be classified under a different category compared to the previous two. It lies between 200ms and 500ms limits and 70% to 80% of the nominal value. The launch of this dip was at the same time instant as the two before.

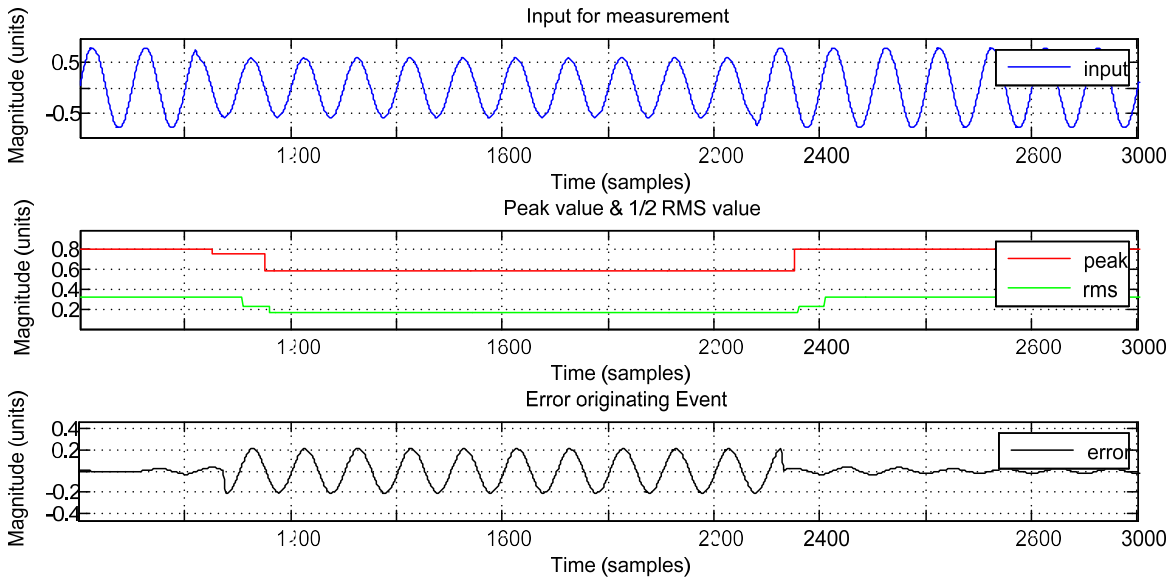

Figure 54 - Results for the detection of dip 3.

Again the positive peak value dropped twice in value. The first drop was due to the partial affect that the dip had on the first positive half-cycle. The abrupt climb in value at the end of the dip indicates that the dip affected one half-cycle completely and stopped being present before the next positive half-cycle. The positive peak value lowered to just below 0.6, 74% of the input magnitude.

The rms value showed a short step at the beginning when the dip was detected as well as at the end, both because half-cycles were partially affected; first the positive one and lastly a negative one when the dip ended.

The magnitude of the error increased in relation to the previous two dips because the difference in magnitude between the measured wave and the generated wave was larger.

Dip 4 was made to have a time length of 550ms and to cause a magnitude drop to 43%. Figure 55 shows the instant when this dip was launched. This dip would be classified under a new group as it would fall under limits between 500ms and 1000ms in length and magnitude between 40% and 70%.

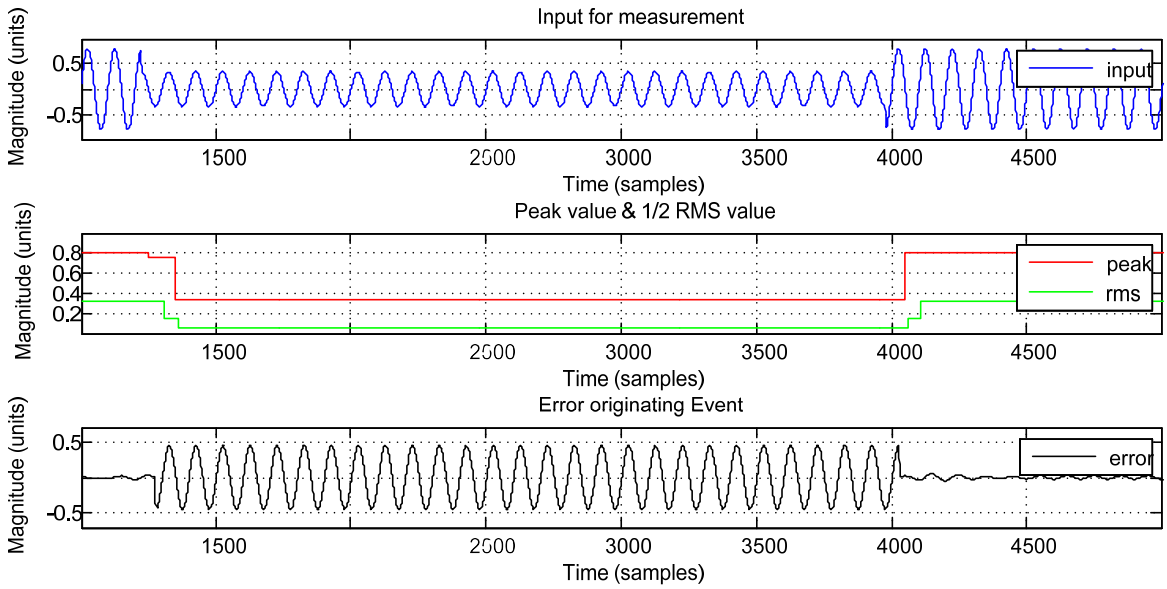

Figure 55 - Results for the detection of dip 4.

The positive peak value had a much deeper drop than any of the cases before. It dropped to below 0.4, less than half of the nominal value. The first half-cycle was only partially affected as in the previous cases. The transition from the dip to the normal value was done in the negative half-cycle. The rms value having intermediate steps at the beginning and the end of the dip period reflects this. The dip persisted for a longer period as can be seen from the x axis. The magnitude of the error increased in comparison to the case before, the dip was also deeper.

Dip 5, twice as long as dip 4 at 1110ms and dropping the magnitude down to 15% was launched at the time instant shown in Figure 56. This dip would fall into a new category, one intersecting the column with duration between 1000ms and 5000ms and row with magnitude between 5% and 40%.

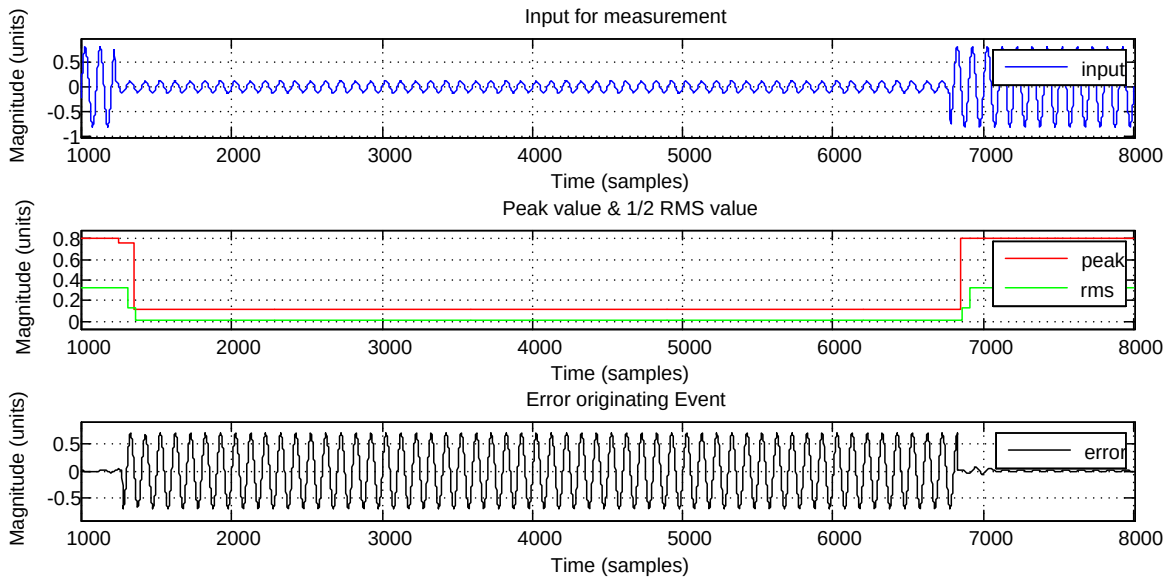

Figure 56 - Results for the detection of dip 5.

The peak value dropped more significantly to below 0.2. Again the first positive half-cycle was only partially affected. The intermediate steps in the rms value indicated that two half-cycles were affected; a positive one and a negative one. The rms value also dropped considerably indicating the aggressiveness of the dip, reflected in the error detected for this disturbance. Although delays were also present as in previous cases, they seemed diluted due to the long time span of the dip.

Dip 6, with a time length almost five times longer than dip 5 ran for 5050ms and dropped the magnitude down to a low 4%, should fall into the last category where the time duration lies between 5000ms and 60000ms and where the magnitude is lower than 5%. Both the initial and end graphs are shown in Figure 57.

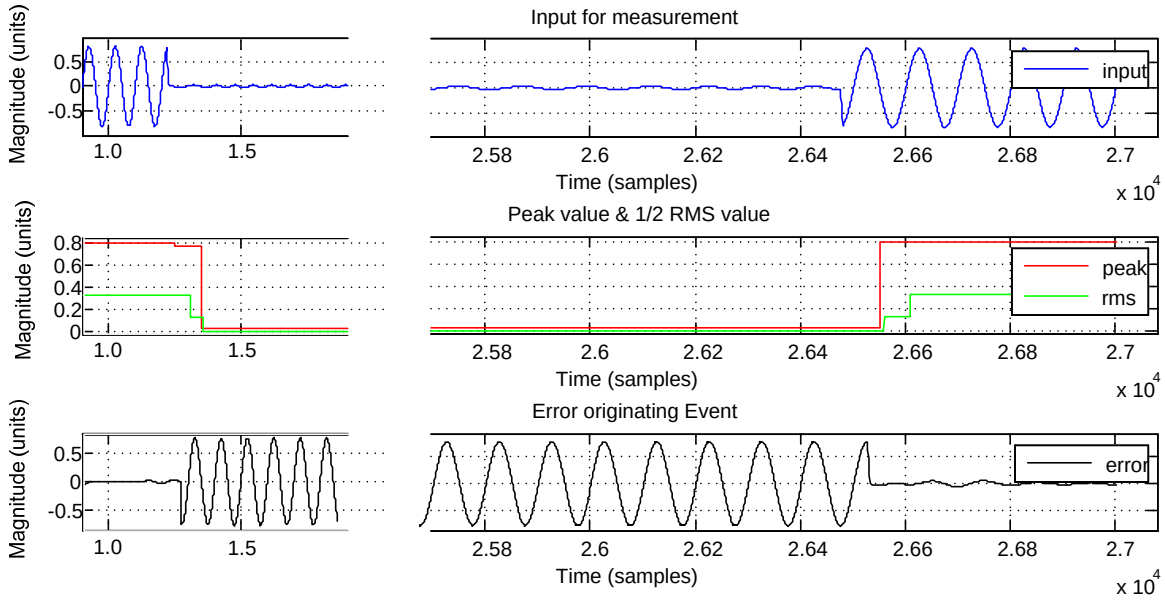

Figure 57 - Results for the detection of dip 6.

The peak value dropped drastically to almost 0%, demonstrating that the first positive half-cycle affected was only partially affected. The recovery occurred during a negative half-cycle, seen in the abrupt increase in positive peak value at the end of the dip. The rms value indicated that both beginning and end of the dip the half-cycles were only partially affected. The error almost reached its maximum because of the difference in magnitudes. In comparison to previous cases the only differences were that the error prevailed for a longer period of time and the magnitude of this error was also larger with respect to the others.

Dip 7 was launched within the time frame as the previous ones, having time duration of 5010ms and dropping the magnitude down to 86%. The results are shown in Figure 58. This particular dip would fall into the category with others of duration 5000ms to 60000ms and magnitude between 80% and 90%.

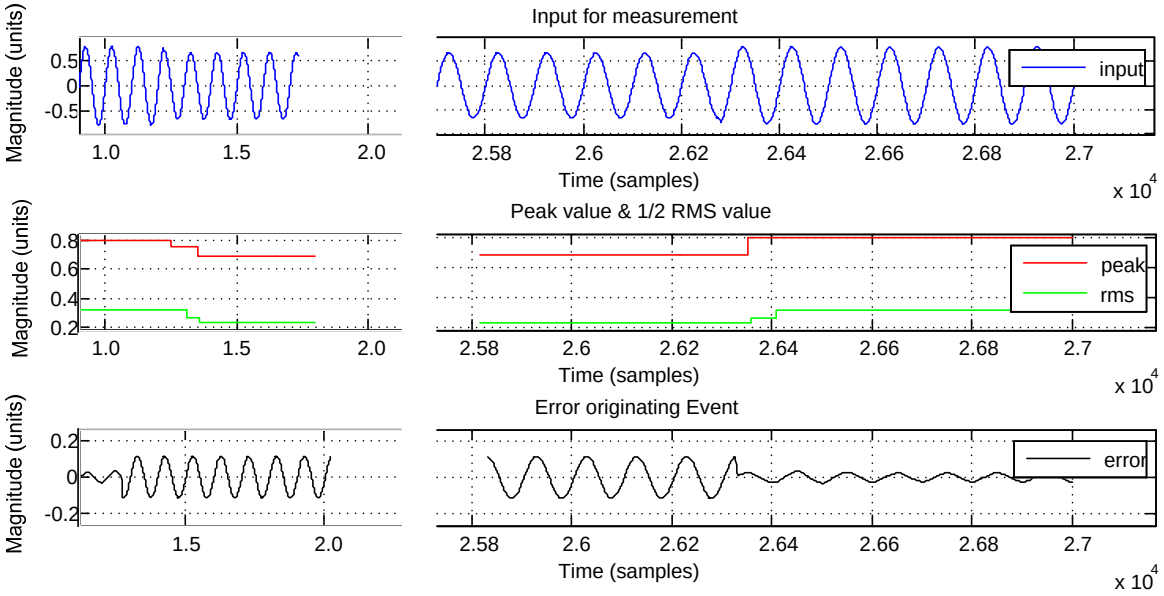

Figure 58 - Results for the detection of dip 7.

The measured peak value showed a slight drop in its value after indicating that a positive half-cycle was first to be partially affected by the dip, as expected. The half-wave rms value indicated that the initial half-cycle and the last half-cycle were both partially affected. The error indicated, by its magnitude, that the difference was not very large.

Dip 8 with length of 1200ms, more closely to that of dip 5, caused a magnitude drop to 77%. Figure 59 shows the results. The classification of this dip would be in the column with time between 1000ms and 5000ms that coincided with row with magnitude between 70% and 80%.

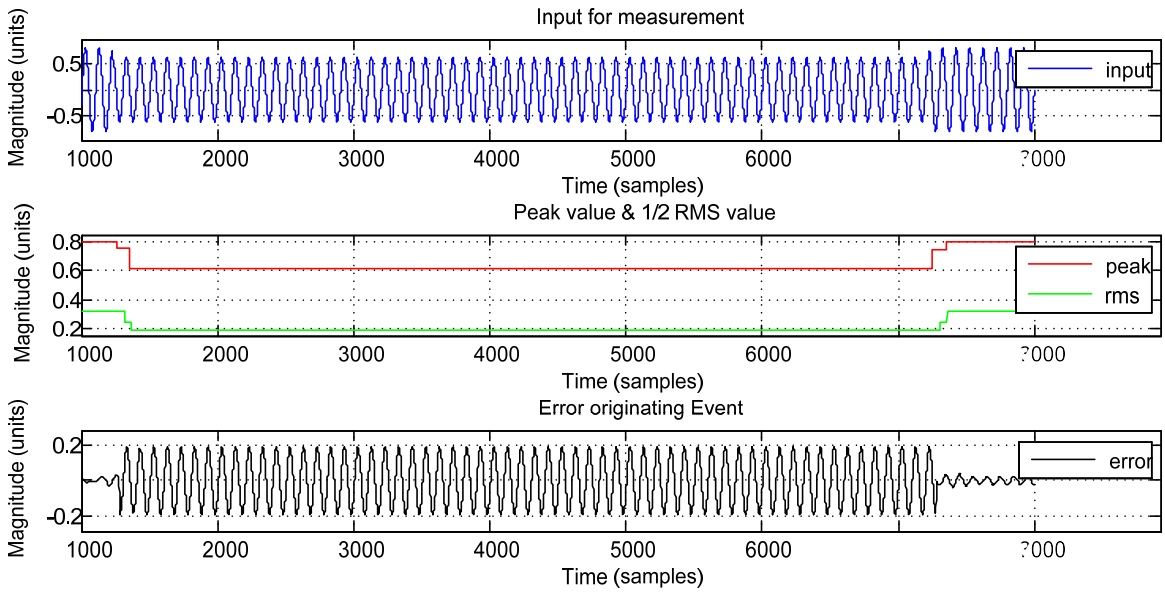

Figure 59 - Results for the detection of dip 8.

The positive peak value measured indicated that two positive half-cycles were partially affected. The rms value correspondingly showed this and the error indicated this respectively.

Dip 9 launched within the same time frame and of time length 420ms caused a drop in magnitude down to 25% shown in Figure 60. This dip would be categorized as one with time duration between 200ms and 500ms and a magnitude between 5% and 40%.

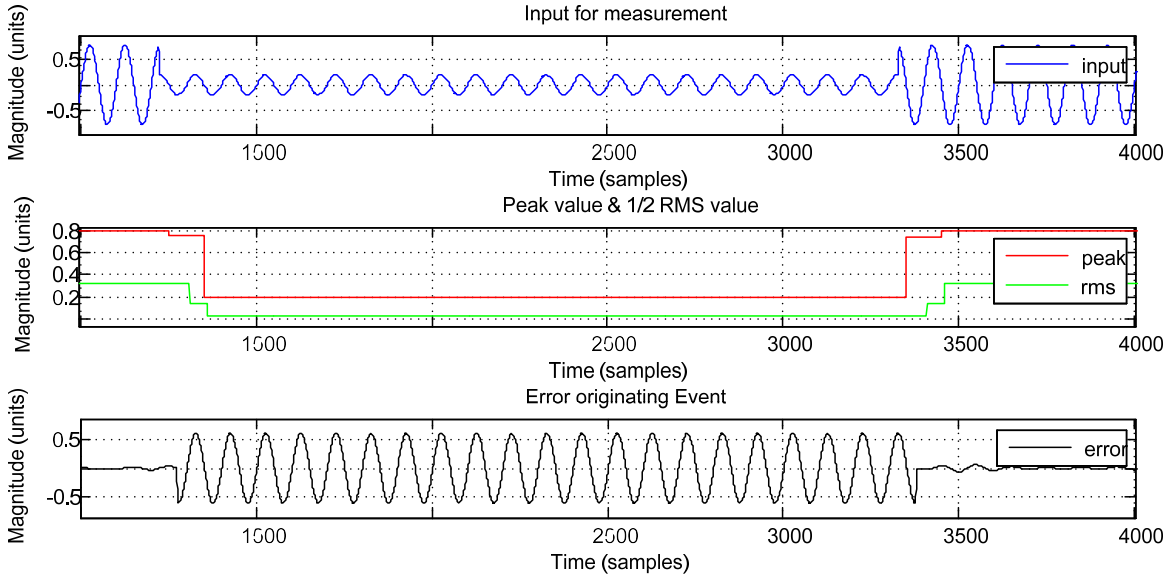

Figure 60 - Results for the detection of dip 9.

The positive peak value indicated that a positive half-cycle at the beginning of the dip as well as at the end were partially affected where the value dropped to approximately 25% of the full magnitude. The half-wave rms value also indicated this decrease and that

two half-cycles were affected at the beginning of the dip and the other at the end of the dip. The disturbance error was large in magnitude.

Dip 10 was launched with time duration of 35ms to cause the magnitude to drop to 2% of the nominal value. Figure 61 shows the results for this simulation. The classification of this dip would be under those of time duration between 10ms and 200ms and magnitude below 5%.

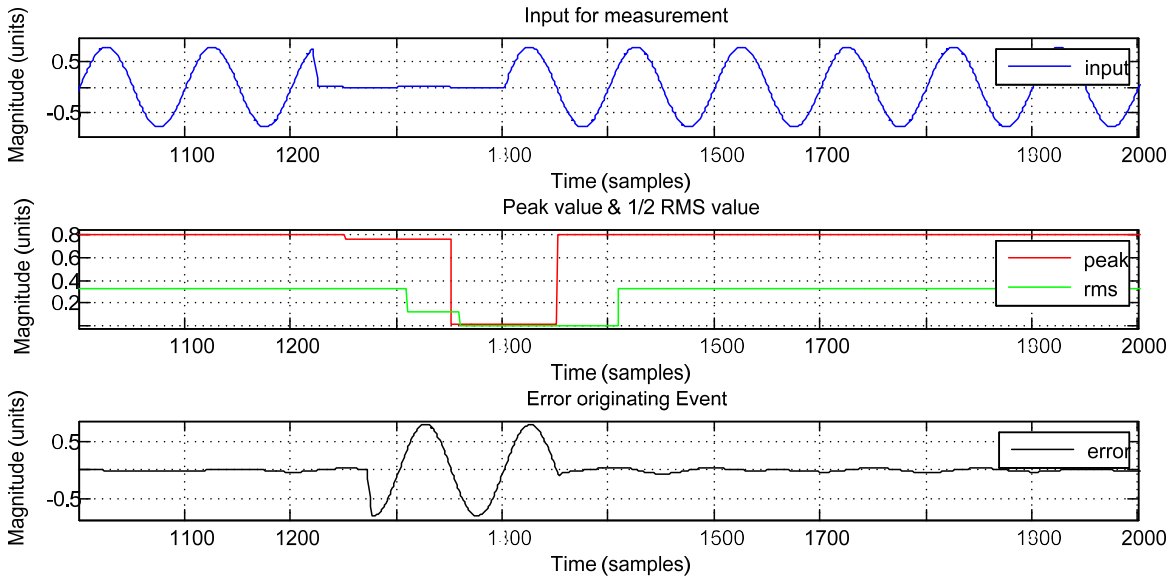

Figure 61 - Results for the detection of dip 10.

The positive peak value registered a stepped drop. The value measured during the dip was almost zero, as could be expected. The half-wave rms value confirmed that the first half-cycle was only partially affected. The disturbance error is very high in magnitude.

In all these cases the frequency continued to be measured and was verified to having maintained at 50 Hz. The full wave rms value followed the values of the half-wave rms with a delay due to the value taking into account the complete value during the wave and not just half of it.

4.4.2. Swells and Other Events

The swells were also simulated according to the European EN50160 Standard. Those chosen for simulations are indicated in Table 15, where each number indicates a different swell used in a simulation. The table only allows for two types of swells; those that fall between 110% and 120% and those above 120%. They are spread over three periods of time.

Table 15 - Swells chosen for simulation according to EN50160.

Swell voltage u	Duration t (ms)		
(%)	$10 \leq t \leq 500$	$500 < t \leq 5000$	$5000 < t \leq 60000$
$u \geq 120$		2	
$120 > u > 110$	1		3

Swell 1 simulated for the duration of 68ms and caused a magnitude increase to 113%. This is shown in Figure 62. This swell would have to be classified as one of duration between 10ms and 500ms with a magnitude between 110% and 120%.

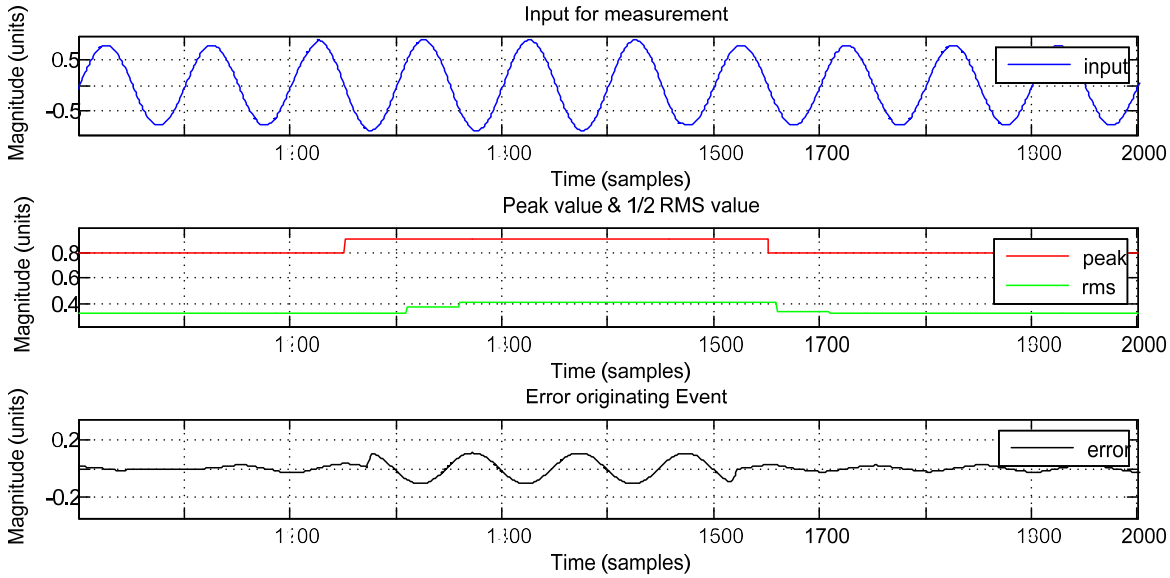

Figure 62 - Results for the detection of swell 1.

The positive peak value increased and the half-wave rms values measurement indicate that also; that the two respective half-cycles were partially affected by the swell. The delays between occurrence in input signal and each result are clearly visible; wherever possible they were kept to a minimum. The disturbance error was relatively low due to the relatively low 13% increase in nominal magnitude.

Swell 2 for the duration of 585ms and causing a magnitude increase to 165%, is shown in Figure 63. This swell should be classified as one with duration between 500ms and 5000ms with a magnitude above 120%.

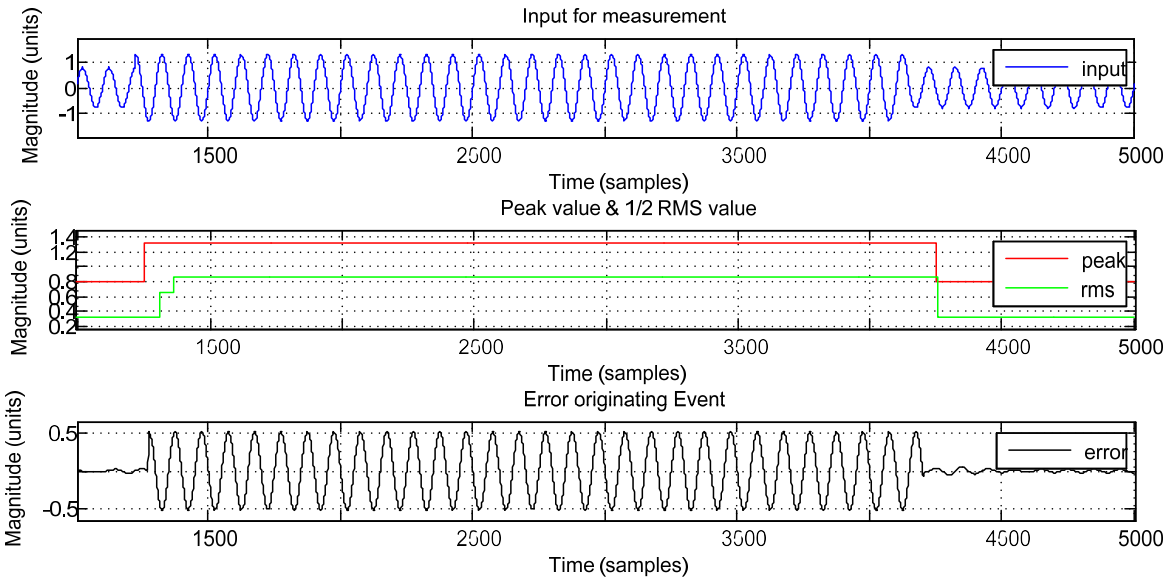

Figure 63 - Results for the detection of swell 2.

The positive peak value noted a large increase. The half-cycle rms value increased beyond 65% due to the value still being the squared version. The square-root function had been removed at the time of simulation. The disturbance error was large as expected since the difference was above 50% of the nominal value.

Swell 3, the one with longest duration of 5010ms and a magnitude increase to 119% was launched after the PLL settling time and is shown in Figure 64. The classification of this third swell should be together with those that fall under duration between 5000ms and 60000ms and provoking a magnitude between 110% and 120%.

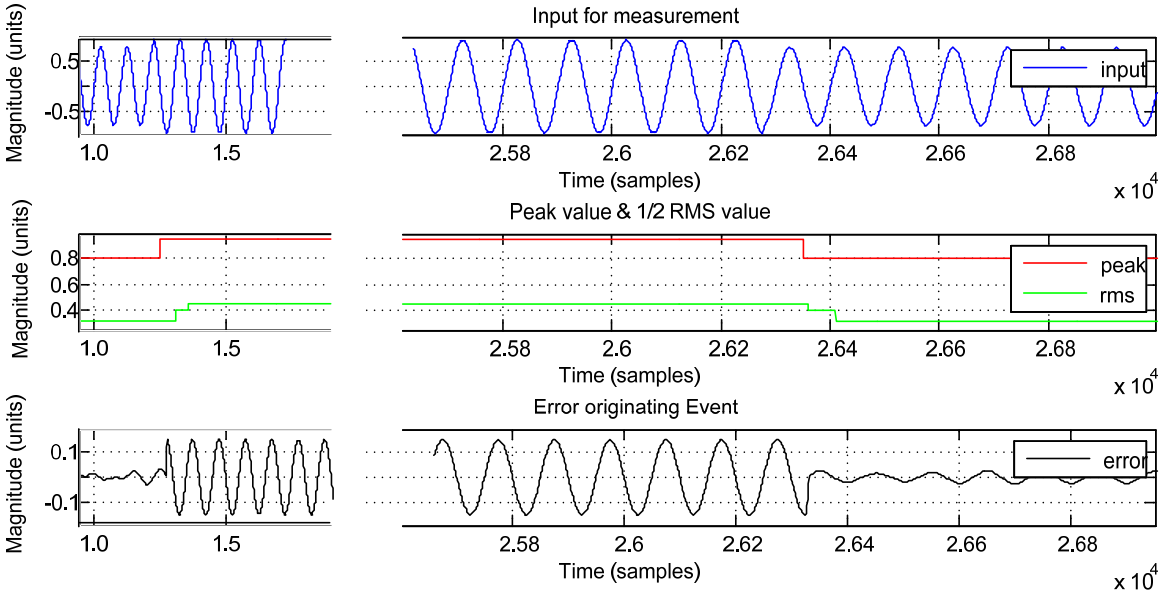

Figure 64 - Results for the detection of swell 3.

The positive peak value increased to a value just under 1. The half-wave rms value indicated that the first half-cycle had only been partially affected with the start of the swell. The last half-cycle during the swell was affected in a similar way. The value during the swell was just under 0.5 due to the square-root function not being used during simulation. The disturbance error was not seen to be exceptionally significant although clearly detected.

In each of these cases the frequency measurements confirmed that the frequency maintained stable at the nominal value. The full-wave rms results were similar to those of the half-wave rms values, with longer delays due to taking into account the whole cycle.

An interruption can be of any length. The one chosen rationally was one with duration 3009ms or, just over 3s. The interruption was initiated with a positive going transient and terminated with a negative going transient as is shown in Figure 65. This interruption would be classified as a short interruption, one shorter than 3 minutes.

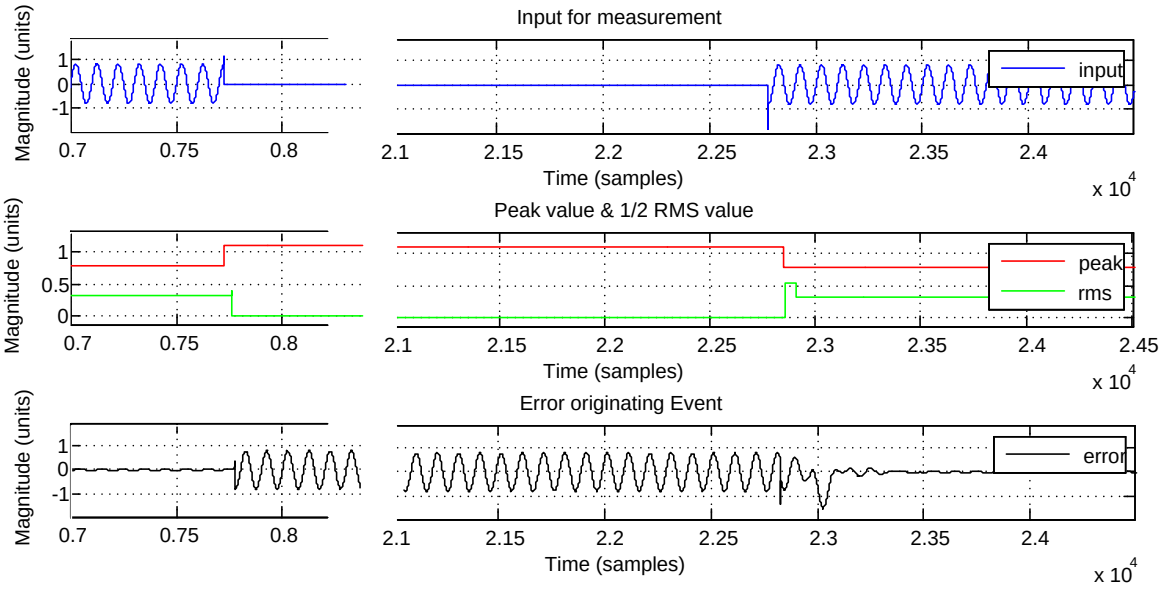

Figure 65 - Results for the detection of an interruption.

The fact that no zero crossings occurred caused all circuits that needed half-wave impulses or end-of-cycle impulses to stop updating. The positive peak value stayed fixed at the last measured value, the positive transient's peak value.

The half-cycle rms value still calculated a value of zero when the positive half-cycle collapsed to zero. A slight increase in value just before this happened was a reflection of the presence of the positive transient. It also calculated a larger value as it recovered due to the negative going transient. It then returned to the expected value for the nominal input signal.

The fact that some values were not updated was advantageous because it allowed the frequency measured to remain at 50 Hz which led to the PLL circuit remaining stable

during the interruption. Additional circuitry would be necessary to create a more robust solution to avoid undesired frequency measurements from reaching the PLL circuit.

The error signal showed that the negative going transient plus the incomplete negative half-cycle disturbed the PLL. The phase-locked loop came to settle around five full cycles later. The transient could also be seen in the measured disturbance error.

A simulation was also done with noise that was arbitrarily chosen. It was launched with a duration of ¾ cycle at t = 0.735s and with a variance of 0.02. This is shown in Figure 66.

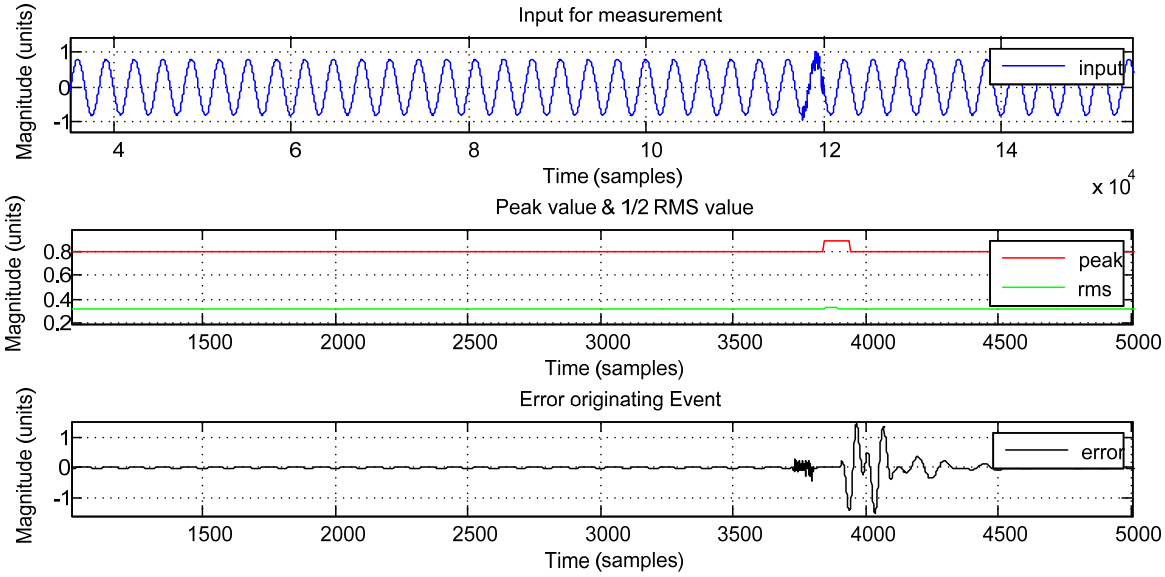

Figure 66 - Results for the detection of noise.

Due to the use of a random number block in Simulink, the number of samples for the input increased in relation to the remaining circuits. The first graph in Figure 48 shows the different scale for the input signal. The peak value measurement reacted to the positive going noise superimposed on the peak of the positive half-cycle when it appeared. The half-wave rms value had such a small increase that it was barely visible, although present. The disturbance error is a reflection of the noise on the input signal. Although the noise was relatively small in magnitude, the zero-crossing was overstepped several times, causing the frequency measurement to be incorrectly done. This influenced the PLL causing it to become unstable. It then recovered after around five cycles.

Two transients were also simulated. These were randomly chosen. Transient 1 was launched at t = 0.324s and having a frequency of around 1kHz. It is shown in Figure 67.

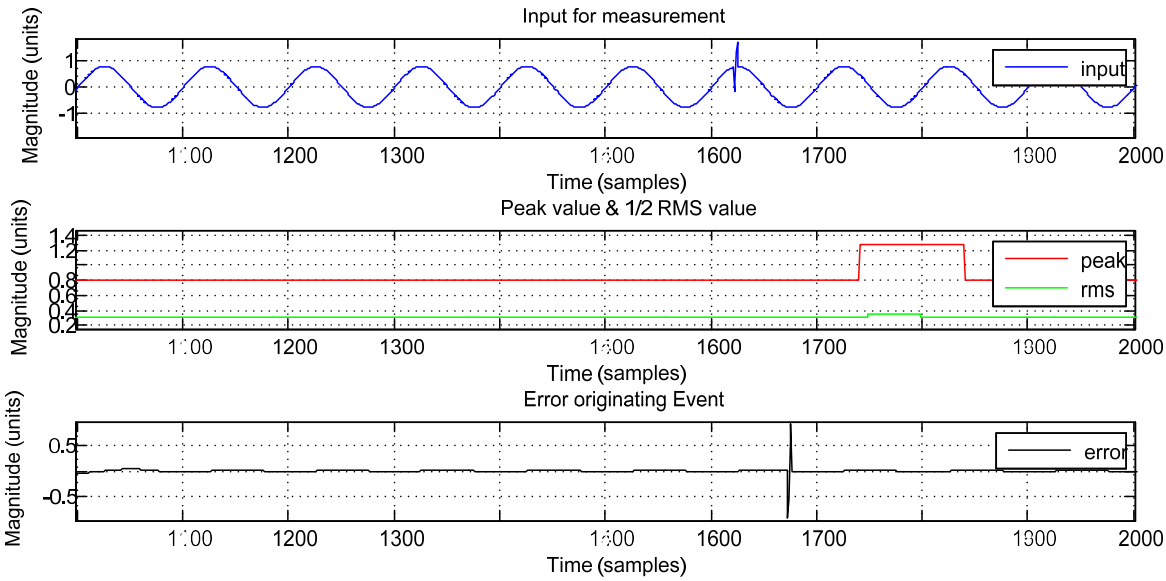

Figure 67 - Results for the detection of transient 1.

The peak value reflected the peak from the transient on the nominal input signal. The half-wave rms value suffered a very slight increase, indicating the small quantity of energy present in the transient. The disturbance error made the transient become evident.

Transient 2 was launched at t = 0.301s as shown in Figure 68. This transient was longer than transient 1 as it oscillated for a longer period of time. It was also made to reappear around 19 cycles later in the negative half-cycle.

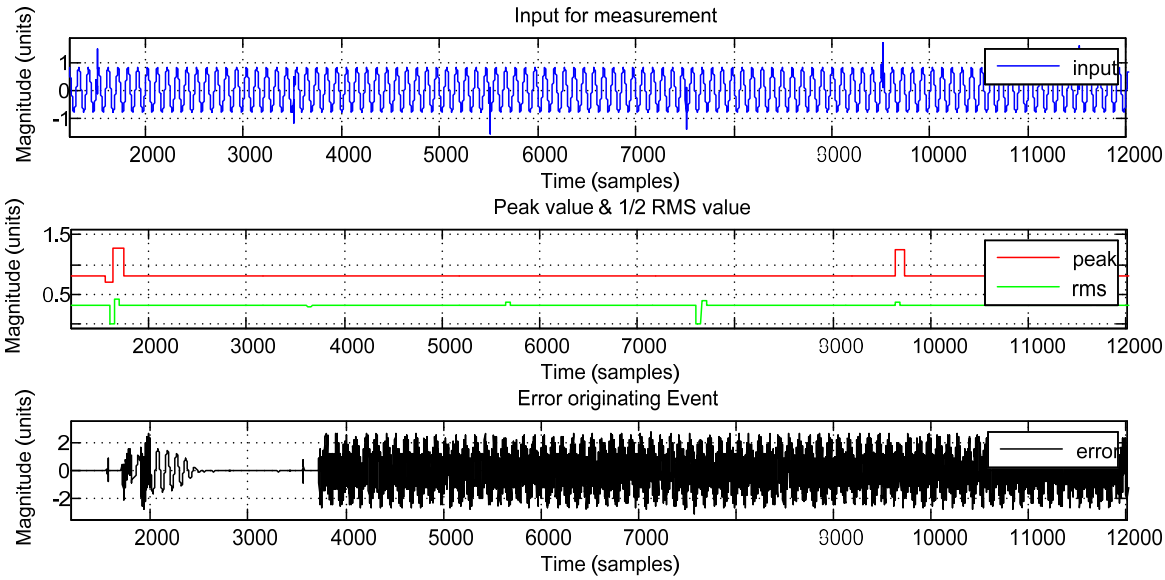

Figure 68 - Results for the detection of transient 2.

The positive peak value detected the transient on the input signal. The second transient in the negative half-cycle would have been detected by the negative half-cycle

peak detection. A small value was detected in the half-wave rms circuit representing the low energy of the transient. Due to some situations of overstepping the zero-crossing during the transient, the frequency measuring circuit incorrectly calculated some values that got the PLL to become unstable. A few cycles were necessary for the feedback loop to stabilize again. During the negative half-cycle transient the PLL circuit was unable to stabilize before a new positive transient appeared. The PLL did not recover till the end of the simulation.

5. Conclusion

This chapter starts by discussing the way that the processing modules could be integrated with the processor and how it could, based on the results obtained by the hardware modules, supply information to the user. It is followed by the principal conclusions of this work and the indication of future work that would be interesting to develop in this field.

5.1. Final Discussion

With the hardware modules supplying the valuable measured values, a processor could be introduced to manage the data. The processor would analyse the data measured by these hardware peripherals to complete the power quality monitoring process. This data could be used to calculate statistics where necessary. Classification of certain parameters would have to be made to meet the latest European Standard. Measurements should be kept in memory for later analysis by the end-user. Important information should be sent to a display that can be constantly updated with new data as it arises.

Presuming that the EN50160 Standard would be used, the processor would have to analyse the measurements and parameters detected according to the limits therein stipulated. Every time a threshold was crossed an alarm flag could be set to warn the user that the specific parameter had been detected and that it had gone beyond the acceptable limits. Depending on the parameter detected data might need to be kept in memory for later evaluation, if needed by the end-user. Other Standards could also be used as a reference for these alarms or even the thresholds set by the user. In this discussion, the threshold values in EN50160 are considered to be the ones used in future.

Although the fundamental frequency measurement should be the aggregated value at every new 10s period, each cycle frequency is also available. The frequency value should be verified to be within 47Hz to 52Hz at any point in time. Should these any of these two thresholds be crossed an alarm flag should be set with a date and time stamp. This could be done as verification on each cycle. An accumulator routine should be used to calculate the frequency average over the time of measurement from when the measurement started to verify if the frequency remains between 49,5Hz and 50,5Hz during 99,5% of the time in a year. A year is a very long time. The decision to warn the end-user before the end of a year is complicated to make. An alternative would be to set a warning flag with time and date stamp if the calculations result in values outside of these thresholds during 99,5% of the time elapsed since the measurement period started. Under normal conditions, where the frequency remains at acceptable levels, this data should be kept in a memory location that is continuously updated as the mirror location of the display to inform the end-user of the frequency at the last 10s interval.

Even though the voltage magnitude should be aggregated as the rms value at every new 200ms period, a half-cycle rms value is also available. This value should also be verified if it is within the expected nominal value to understand whether or not there is any waveform deformity. The processor would have to verify that the rms values are within 207V and 253V during 100% of the time even though the standard indicates that it should be only during 95% of the time. Another lower threshold at 195.5V should also be set to alert the end-user that the -15% tolerance has been reached in islanded systems not interconnected with transmission systems. This later threshold should be an optional function only to be used if the user so desires. The respective alarm flags should be set if necessary for each of the thresholds and saved to memory with date and time stamp.

Harmonics should be verified by the processor. Should any harmonics be detected an alarm should be set and the data saved with time and date stamp for later evaluation. The processor should also analyse each of these harmonics to verify that they do not exceed their individual limit. If any one of them does, the respective alarm should be set and data saved to memory to be evaluated later. The processor should calculate THD by adding the magnitudes of all harmonic components up to the 40^{th} order to see that the total is not higher than 8 % of the fundamental magnitude value. If this value is superseded the respective alarm should be set and the data saved with time and date stamp. A second THD could be calculated up to harmonic order 50. All harmonic related data should be updated to the display as well.

Even though there is no real definition for inter-harmonic component content, these values should be verified by the processor. These values could then be supplied to the end-user as a block of values between two harmonic components in a type of list with around 38 values. A Total Inter-harmonic Distortion (TID) could be calculated somewhat similar to THD up to harmonic order 40. A second TID could also be calculated for inter-harmonic components up to harmonic order 50. Only TID values should be sent to the display as informative values. Should the end-user then require it, the listed data could then be supplied.

Mains signalling would have to be verified by the processor according to Table 16 which reflects the data from the figure from the standard for mains signalling.

Table 16 - Mains signalling values.

Frequency Range	Percentage Voltage Level
100Hz – 500Hz	9%
500Hz – 950Hz	Ramp from 9% to 5%
950Hz – 9.500Hz	5%
9.500Hz – 100kHz	Ramp from 5% to 1.133%
95kHz – 148.5kHz	$< 1.4V_{rms}$

The verification that should be done over a 3s moving window period is that the values of inter-harmonic values between each frequency range are equal to or below the percentage voltage level. If these values are exceeded an alarm flag should be set and the

alarm saved to memory with time and date stamp. Whichever values are measured during the 3s period, the data should be sent to the display and saved to memory with time and date stamp.

Rapid voltage changes are clearly defined in the European Standard, the processor should look out for this phenomenon. It should have a first set of thresholds set at 218.5 V and 241.5 V, equal to the 5% tolerance indicated in the standard, and a second set of threshold values set at 207 V and 253 V, equal to the 10% tolerance in the standard. The half-wave rms value could be used for this verification as a new value is available at every new half-cycle. If a fast change in value should be detected, the alarm flag should be set and a period of information before and after this happening saved to memory with time and date stamp after verification that this is not any other type of event. Every time the value falls within the last set of thresholds yet outside the first set of thresholds, an accumulating counter should be incremented to indicate the amount of times a day this occurred. Every time the value falls only within the first set of thresholds its respective accumulating counter should be incremented. The respective saved data should also be identified accordingly for later evaluation. The respective data should also be sent to the display and kept updated.

Dip threshold values should be set by the processor at 11.5 V and 207 V. As soon as the half-wave rms value falls below 207 V a dip alarm flag should be set and data recorded from one or two cycles before and during this event with time and date stamp. If the dip does not reach 11.5 V and returns to the nominal magnitude value, the only task that still has to be performed is to classify the dip according to the table in the standard and update the dip classification table. Should the dip value go below 11.5 V, then the dip flag should be reset and the interruption alarm flag set. The data should be kept as was already the case for the dip and the interruption duration measured. The corresponding data should be sent to the display. Care must be taken to make sure that the dip classification table is only updated after the event has terminated.

The interruption should be analysed as just mentioned. Two accumulating counters can be used to supply the statistic to the user; one for the number of interruptions shorter than 3min and a second one for the number of interruptions longer than 3min.

Swell threshold values should be set by the processor at 253V and 276V. As soon as the half-wave rms value is larger than 253V a swell alarm flag should be set and data recorded from one or two cycles before and during the event, with time and date stamp. If the swell does not reach 276V and returns to the nominal magnitude value, the only task still to be performed is to classify the swell in the swell classification table and update that table according to the standard. Should the swell exceed 276V, the swell alarm flag should be reset and a transient alarm flag should be set. The corresponding saved data for the swell becomes saved data for the transient until the event ends. Care should be taken to update the classification table only after the event has ended.

Transients have therefore just been dealt with. A separation of transients could be made distinguished by their rise time. With the sample resolution used, this should be

possible; μs rise time is usually a transient caused by lightning while ms rise times are usually caused by switching.

The end-user would be able to look at the display at any time during the measurement period to see the dynamic measured values or values present at that instant. Only after the measurement period has terminated or forced to stop by the user, should the user be granted access to the saved data and alarms. The user should be able to enter a menu to select the type of event he requires to evaluate. After selecting the type of event, by moving a cursor over the events indicated by the time and date stamp, he should then be able to select them. The display would show the "photograph" of the event.

A second form of access should also be granted by PC through a RS-232 or USB connection, depending on the interface used, via the FPGA UART where all data could be downloaded to be visualized on PC. A graphical program would assist in the viewing of the event "photographs".

5.2. Main Conclusions

The system implemented includes units to measure various site indices, harmonic and inter-harmonic components and events. The site indices are: a) fundamental frequency; b) positive and negative peak values; c) full wave and half-wave rms values, while events are: a) dips; b) swells; c) short and long-term interruptions; and d) transients. The system frequency measurement resolution at 50Hz is 0.0031Hz while the resolution of the magnitude measurement is 0.009V.

It is evident from the results that with the FFT unit all harmonic components up to and including order 50 can be captured. This applies to respective inter-harmonic components also where nine inter-harmonic components are available between every two harmonic components when a bin footprint of 10Hz is used. A larger separation will cause excess of information to become cumbersome to deal with. With the zero-crossing fundamental frequency measurement, the comparison can be made to verify with a high degree of detail that the frequency measurement is correct. The mains signalling communication can be sifted out with the use of a second FFT so that harmonic and inter-harmonic component content can be easily separated from the mains signalling data. Aggregation statistics of these values can be kept in memory when the full amount of data is not needed.

With the high resolution results in the peak value measurements, rms and half-wave rms calculations, highly accurate measurements can be achieved in the signal measurements and any slight positive or negative fluctuation in the magnitude will be detected.

Results show that the PLL unit produces an authentic imitation of the ideal input against which the true input is compared allowing every deviation, however small, to be

extracted for the correct post analysis by the FPGA processor. Due to the FPGA speed this analysis is almost instantaneous or in real-time.

It is safe to conclude that the solution chosen can be used for the analysis of power quality and the problems associated to it. In some cases the resolution obtained with the high sample rate is superior to the two instruments that were evaluated. This would have the advantage of better defined fast events on the waveform where quality of image is necessary. Extra-fast phenomena would have more difficulty to go by undetected. More work is necessary to complete the range of parameter detection and measurement.

The conclusion is that this FPGA is a feasible solution for the implementation of a reconfigurable power quality monitor. The FPGA alone has more than enough capacity to deal with all the necessary measurements, making high resolution analysis and visualization possible. The FPGA structure makes it possible to add a variety of future functions that have not even been thought of yet, without the need to alter any hardware. This makes the reconfigurable power quality analyser very versatile in the future to come.

It is also possible to conclude that the System Generator tool, run on the Simulink/Matlab platform, make it possible to develop all the hardware necessary to implement the reconfigurable power quality analyser in the FPGA, with less effort than it would be necessary if a hardware description language was used.

5.3. Future Work

Future work would necessarily include the integration with the processor, which would be responsible for the end-user interaction. It should aggregate data that is not already aggregated in hardware and complete decision tasks. According to the end-user requirements it should supply data to the on-board screen. When required it should liaise between the end-user's PC and memory through its peripheral UART interface. Predefined configurations such as those from EN50160, the unified method in IEEE 1149 and the classic method from the IEEE 1459 standard could be preconfigured. The user should be able to define other threshold values if desired.

The implementation of an analogue front-end board would also be mandatory, with an interface to the FPGA development board used. This would allow the system to be tested with real signals in order to evaluate its performance. Beyond this, further work could also be done to enhance the implemented digital processing module, as described in the following paragraphs.

The system could also be modified to mitigate spectral leakage. For that, it would be necessary to include a buffer just before the FFT, to temporarily keep the wave samples. This buffer would only be filled with samples for complete integer cycles. If the next cycle has more samples than the samples still available in the buffer, this remaining space should be filled with zeros. Upon full, this data would be available to the FFT. In so doing no cycle would be lost and spectral leakage would be reduced to a minimum.

A low-pass filter to remove all the harmonic and inter-harmonic components could be introduced before the fundamental frequency, peak values and the rms values are measured and calculated according to the indications in the standard that this should be done.

A THD calculator could be implemented in hardware to include harmonic components up to order 40 and up to order 50. An equivalent calculator could also be implemented for the inter-harmonic components.

The flickermeter according to IEC 61000-4-15 should be implemented. This would allow the processor to collect the short-term severity (Pst) value from the flickermeter at every 10min and send it to the display. This value should be kept in memory until 12 values are saved and added together. The long-term severity (Plt) should then be calculated for the respective 2h period and sent to the display. Should this later value be equal to or superior to 1, an alarm flag should be set and the data stored in memory with time and date stamp for further evaluation by the end-user, when requested. The 12 Pst values could be kept to understand which specific 10m periods had exceeded values or for how long these were present.

If it is presumed that the first measurement subsystem (this project) is destined to voltage measurements, a duplicate of this subsystem should be used to measure all phenomena for current simultaneously. The same measurements could be made.

If it is presumed that these two subsystems would complete the single-phase voltage and current measurements, four of these units should be used to measure all phenomena for the three-phase systems including neutral. In this situation, the same measurements would be made but some others would be necessary, which make sense for three-phase systems only (such as unbalance detection).

The introduction of the flagging concept, power calculations, power factor and inrush currents could also be made. The flagging concept already explained in other sections is ideal to alert the end-user that limits have been exceeded and that these limits have not been identified as more than one disturbance at any one time. Power calculations can help the end-user understand at that very moment how much energy is being consumed. Power factor values will help the end-user understand if there is an existing problem with reactive power, inductive or capacitive caused by the installation on the electric grid. Inrush currents will allow the end-user to understand how the transformer affects the electric grid every-time it starts up from a power failure. This is all very useful information for the end-user when doing diagnostic checks.

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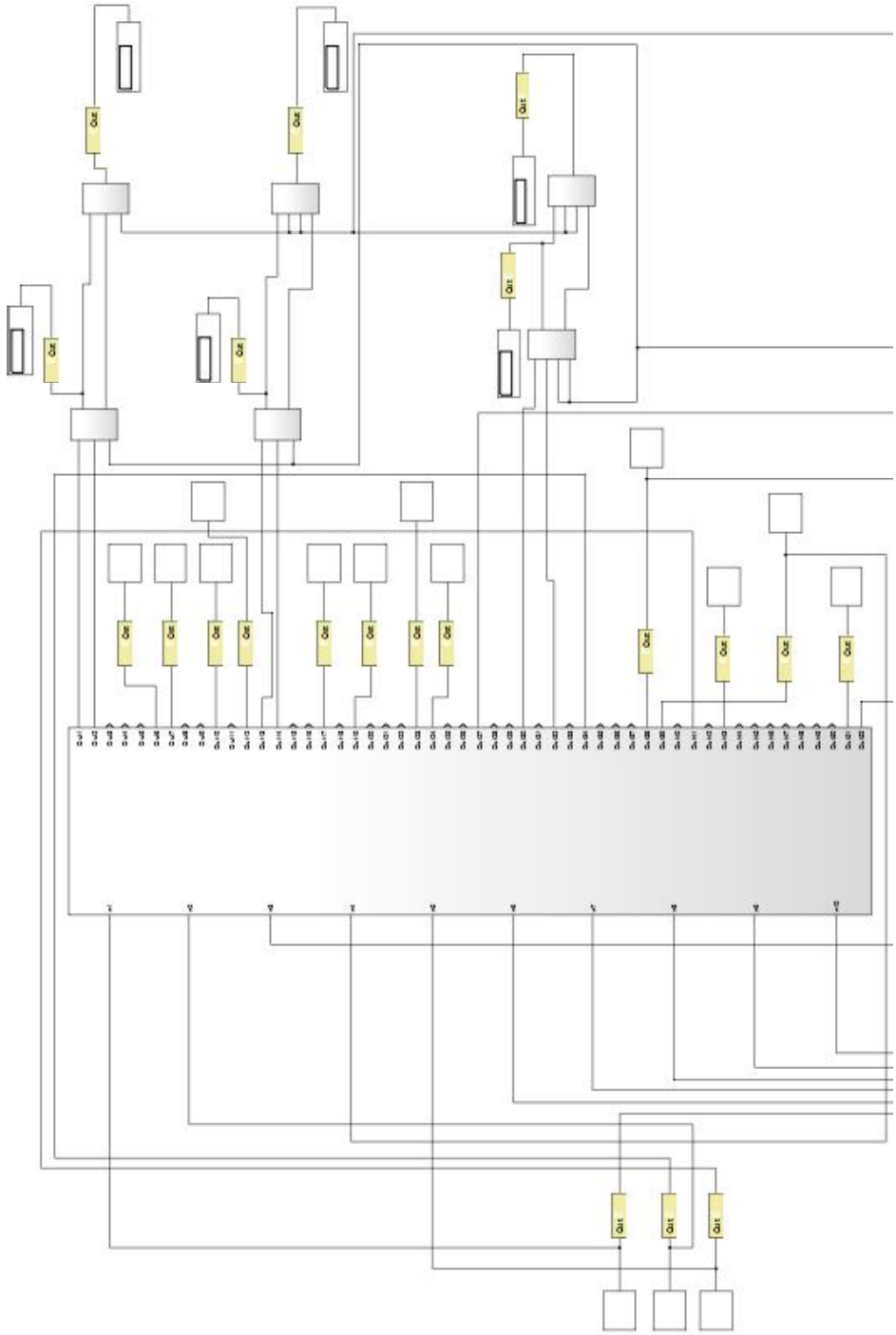
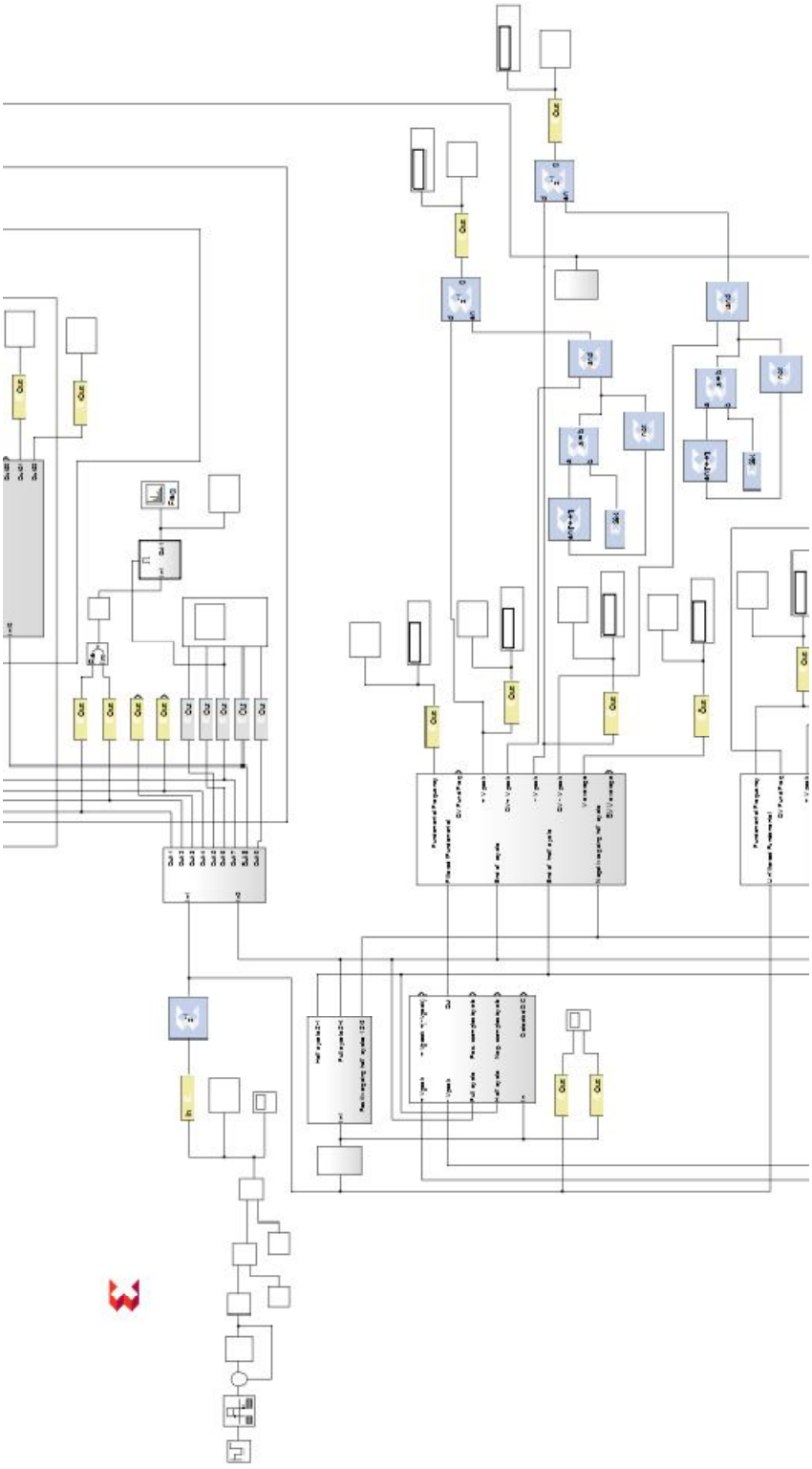
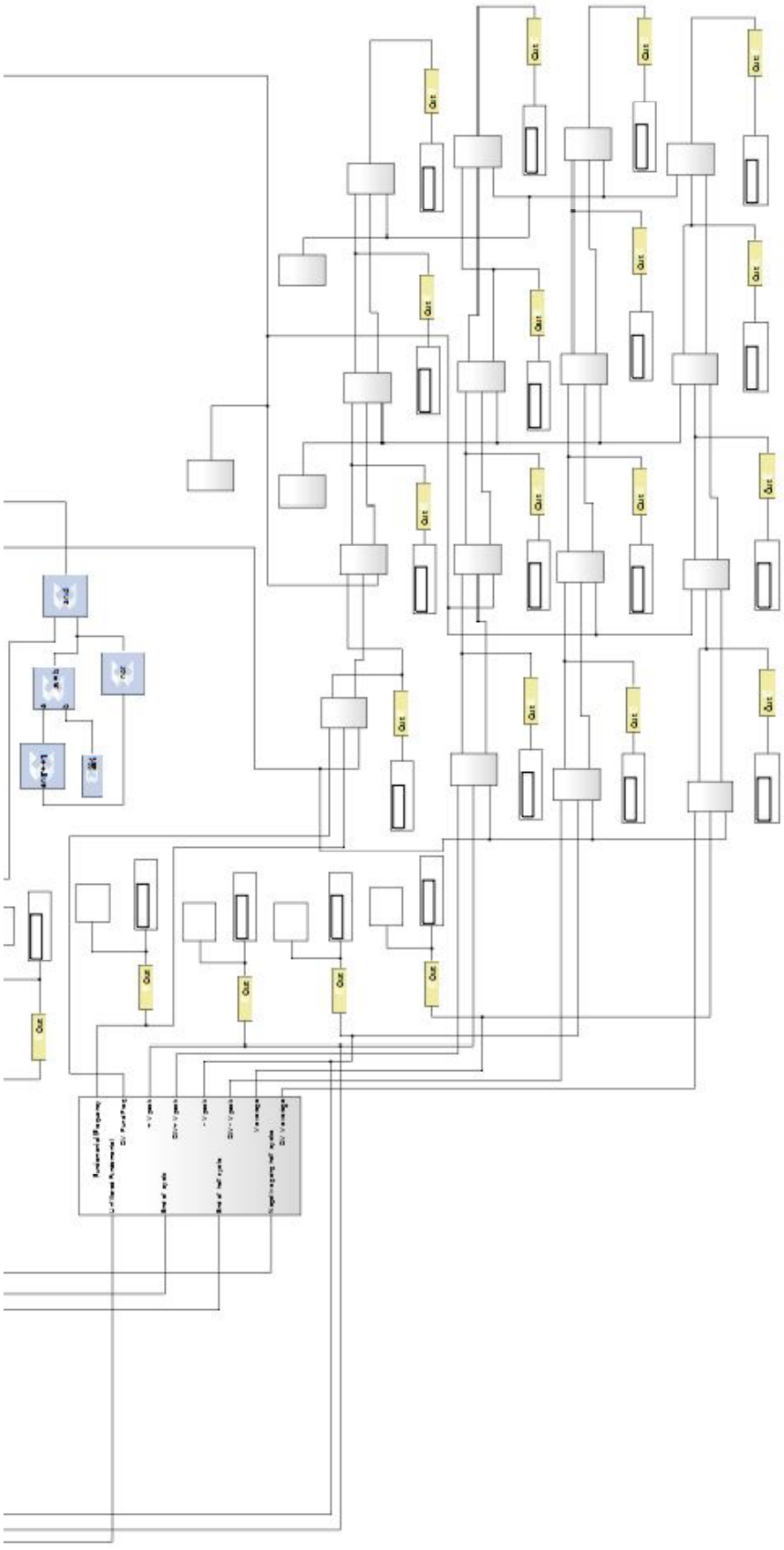
Annexes



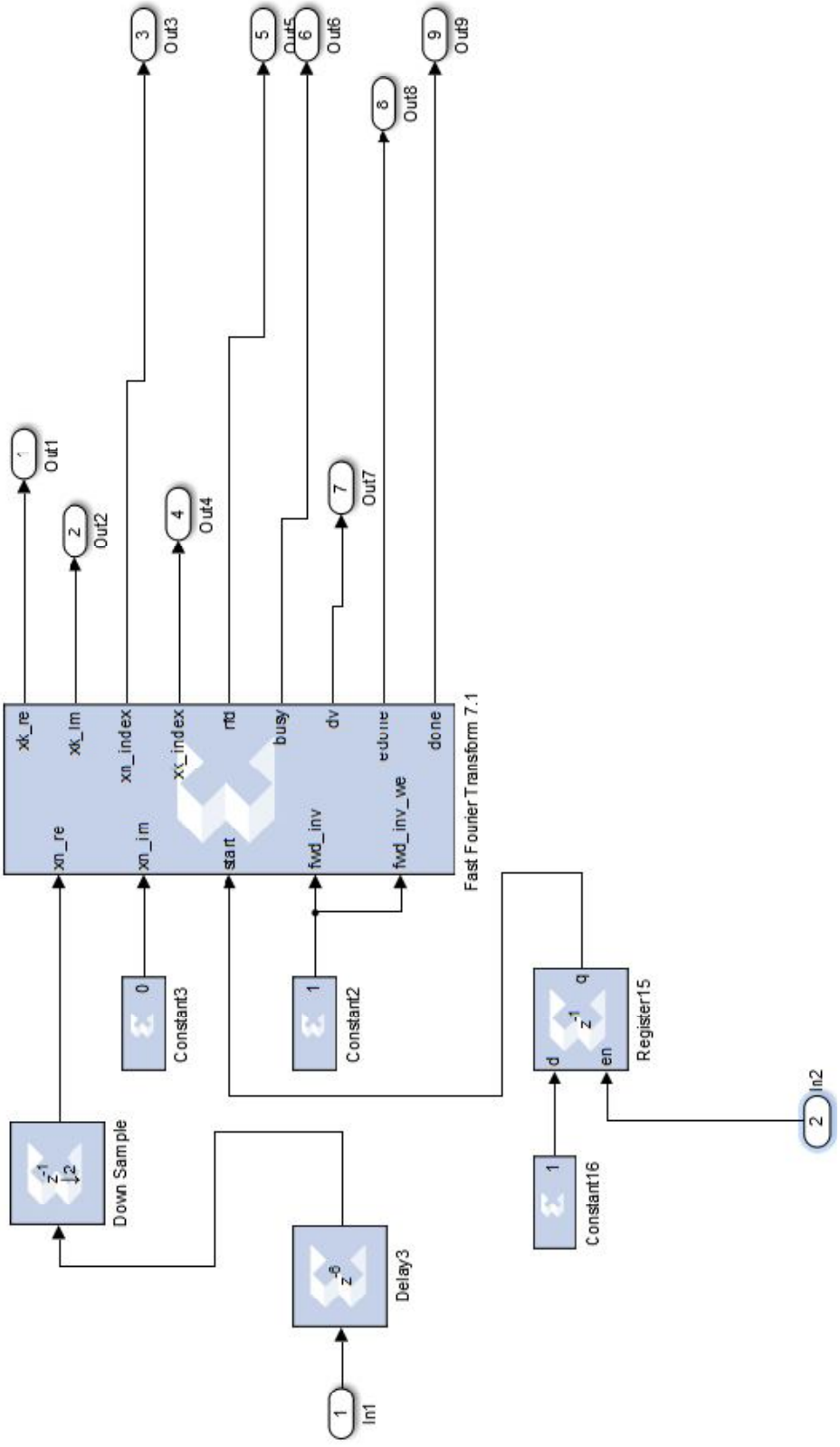
Annex 1 – FFT full system part 1.



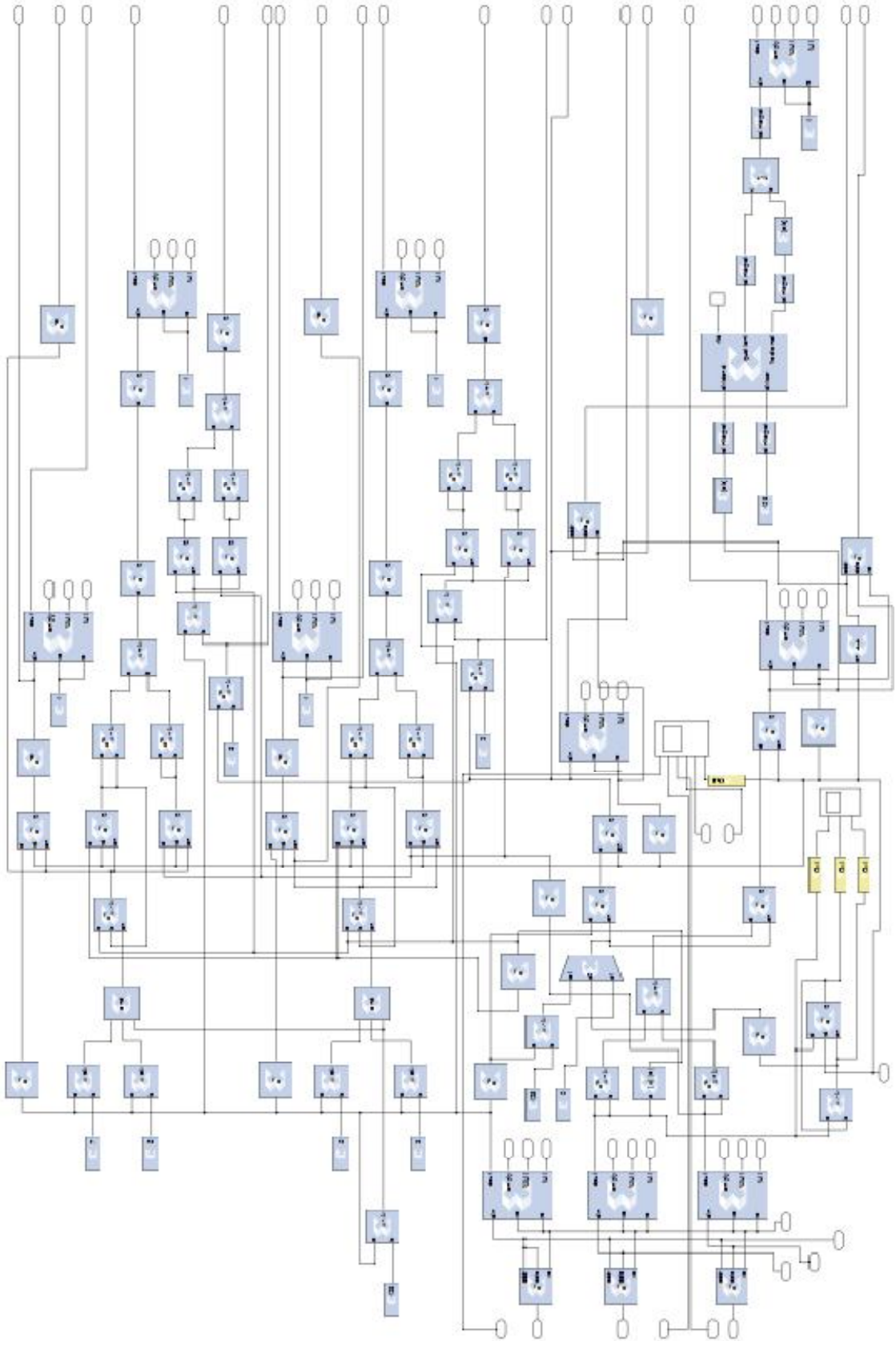
Annex 2 – FFT full system part 2.



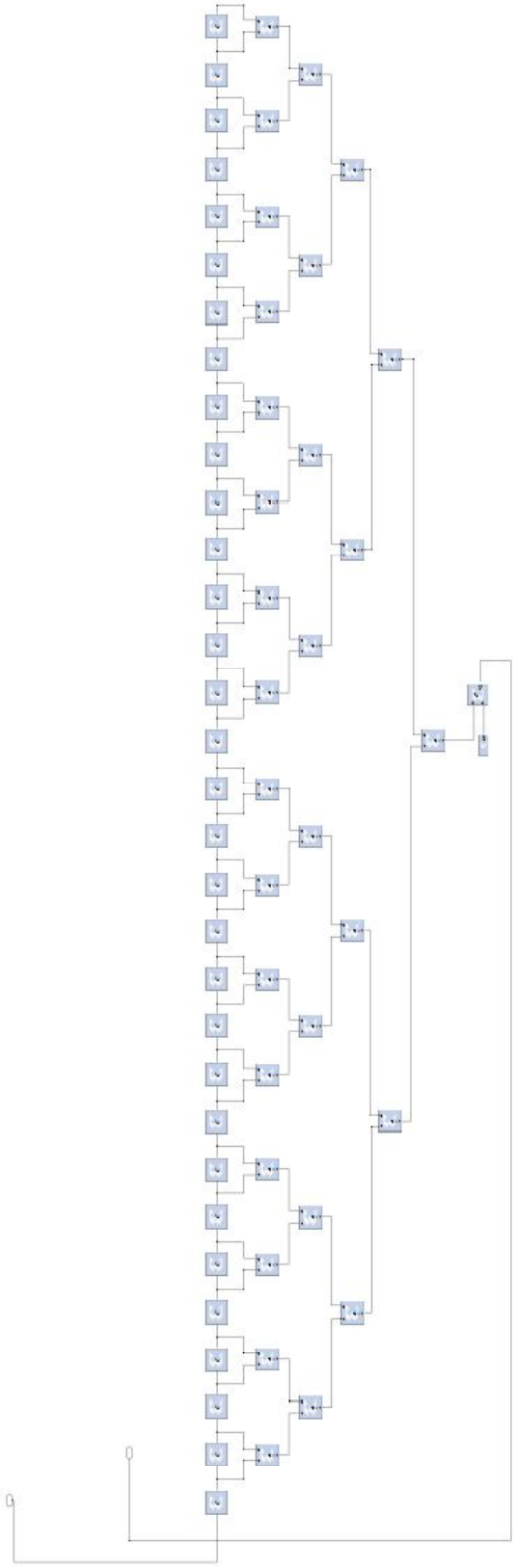
Annex 3 – FFT full system part 3.



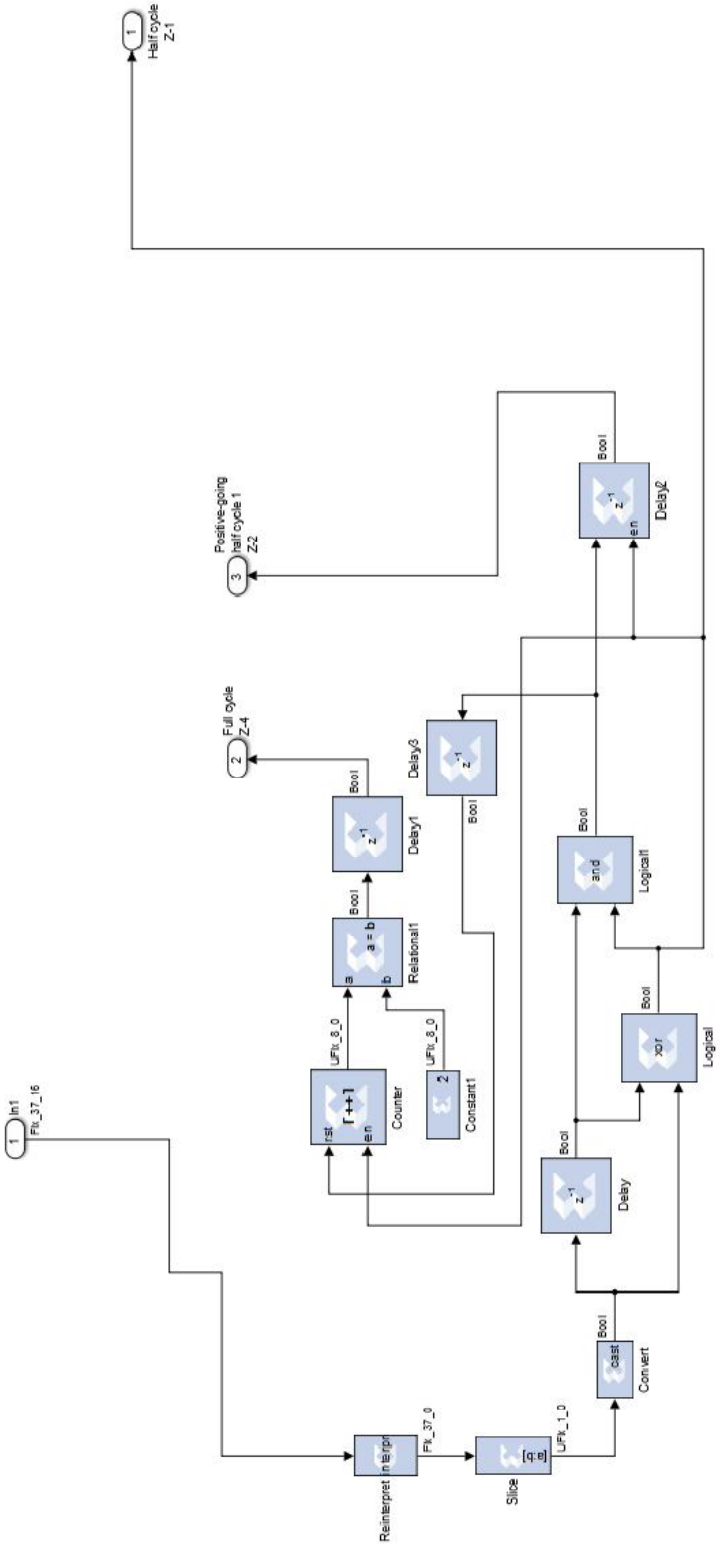
Annex 4 – FFT subsystem.



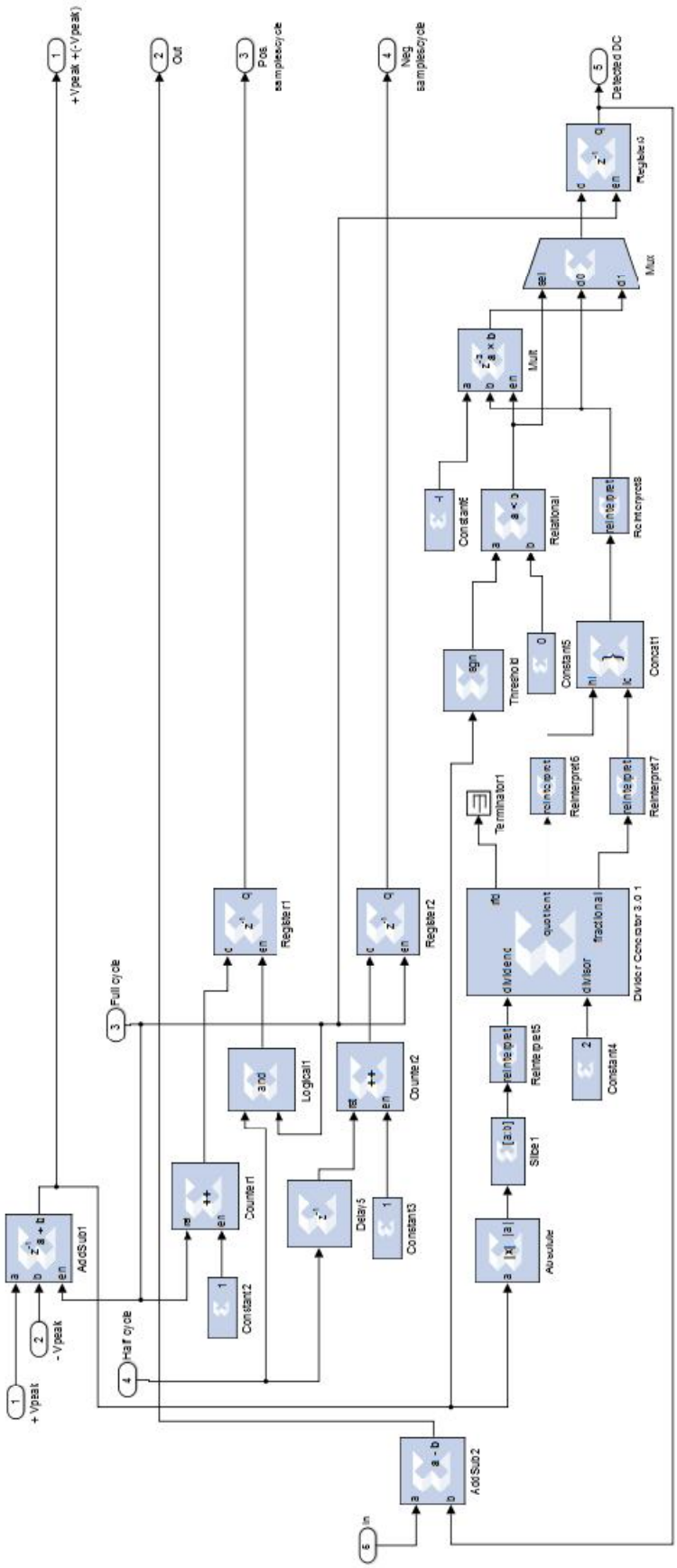
Annex 5 – Power spectral analyser subsystem.



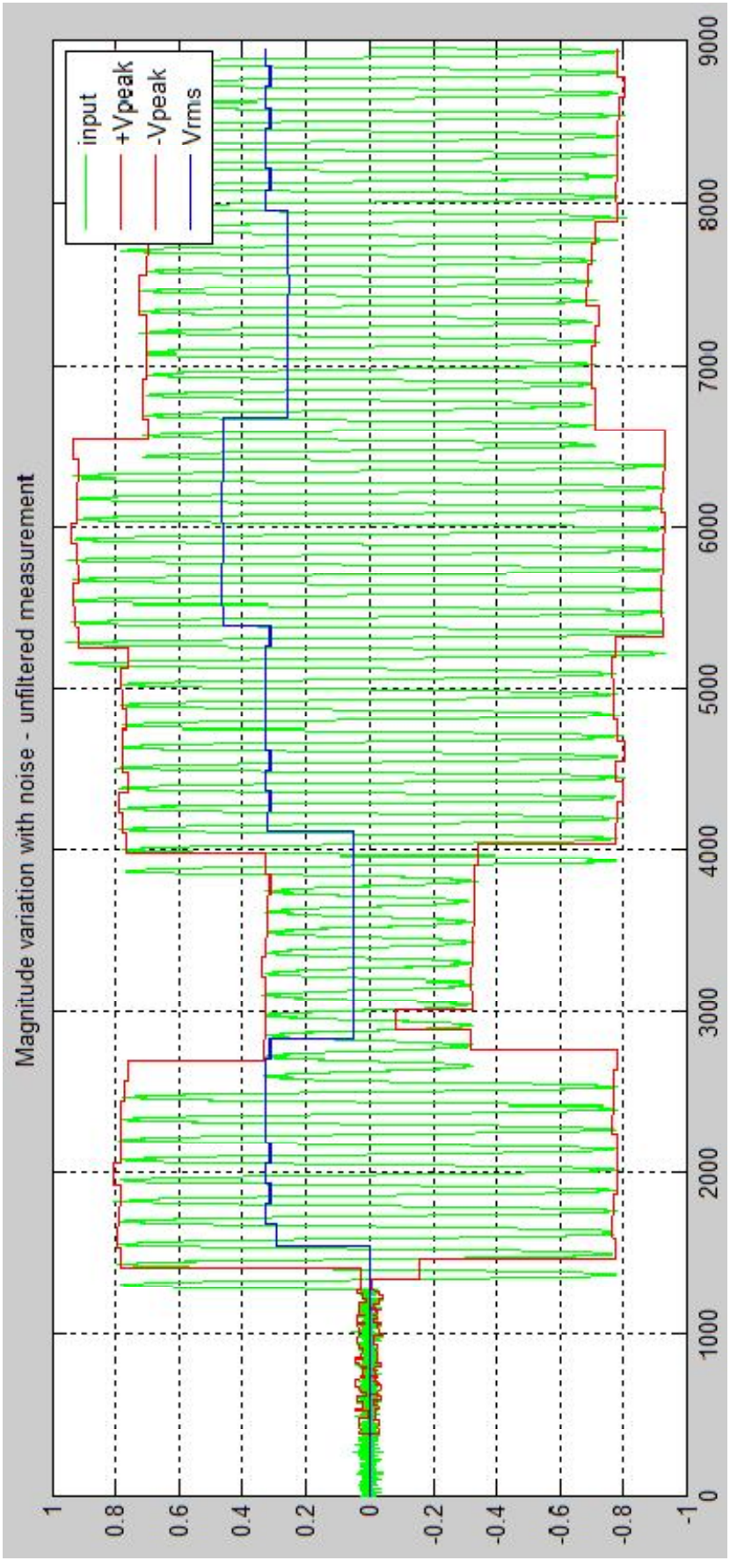
Annex 6 – Moving average filter subsystem.



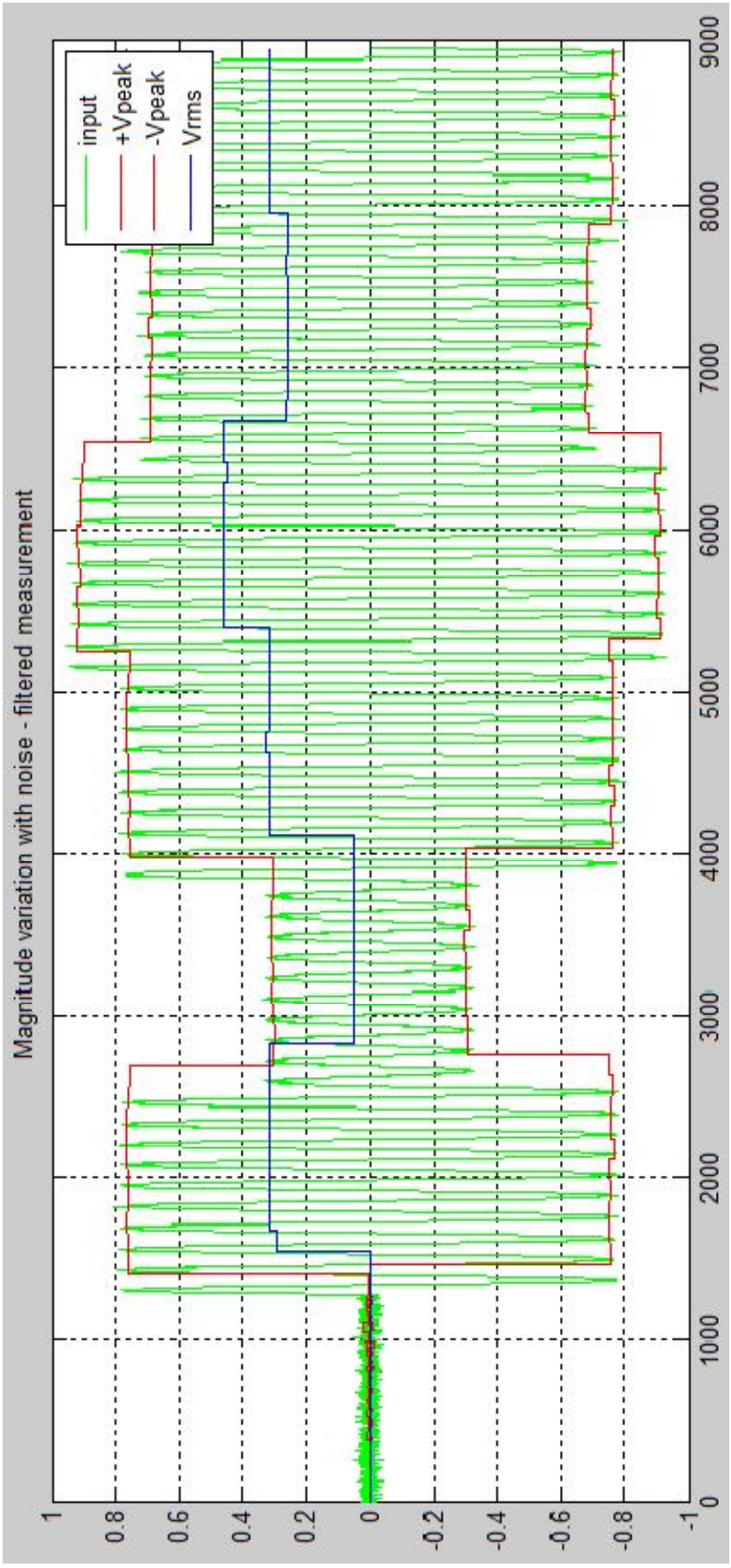
Annex 7 – Zero-crossing detector subsystem.



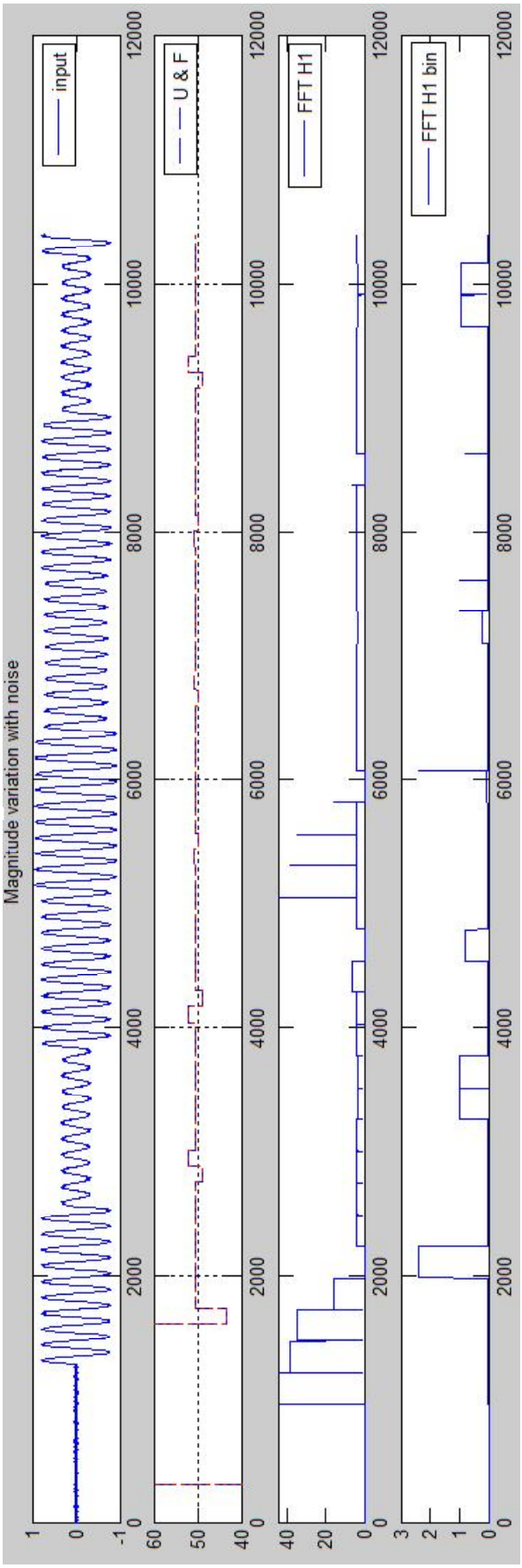
Annex 8 – DC blocker circuit.



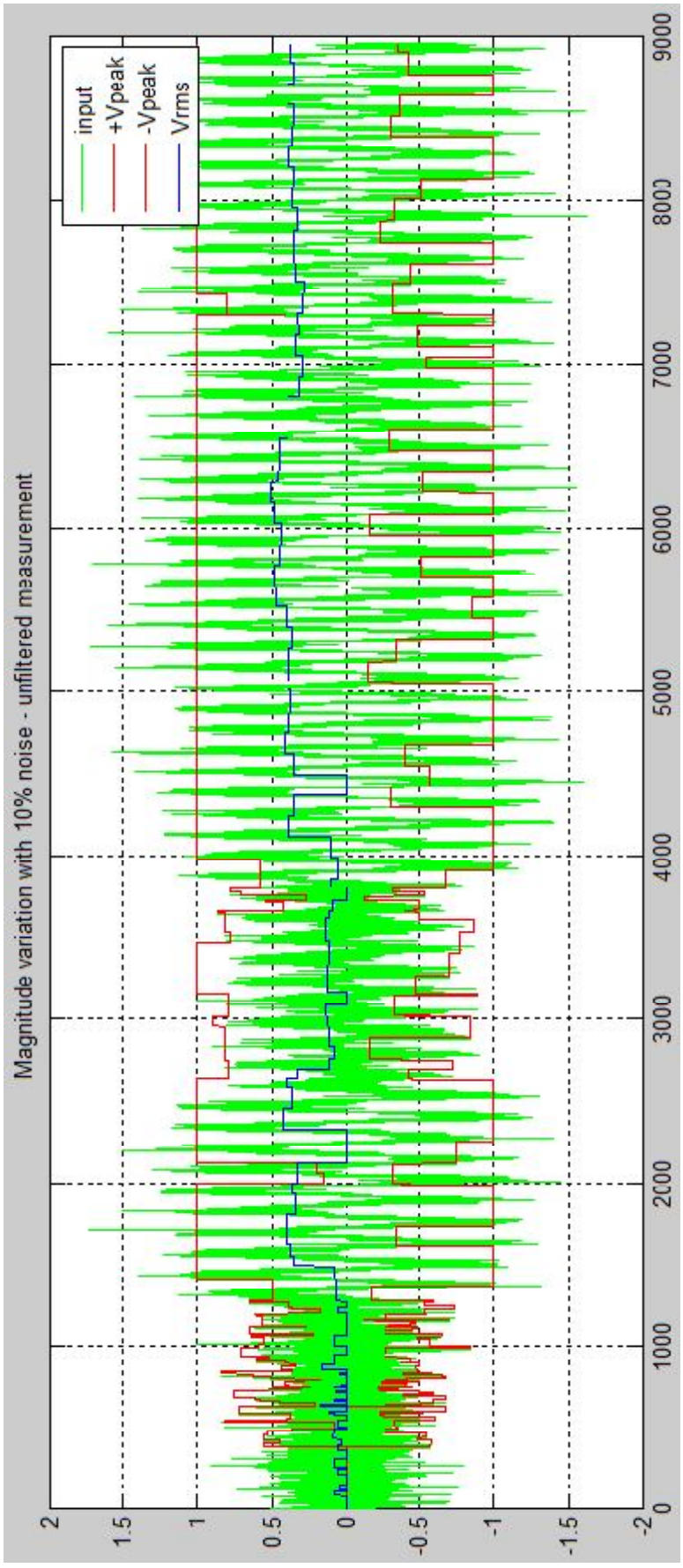
Annex 9 – Magnitude variation with noise and unfiltered measurement.



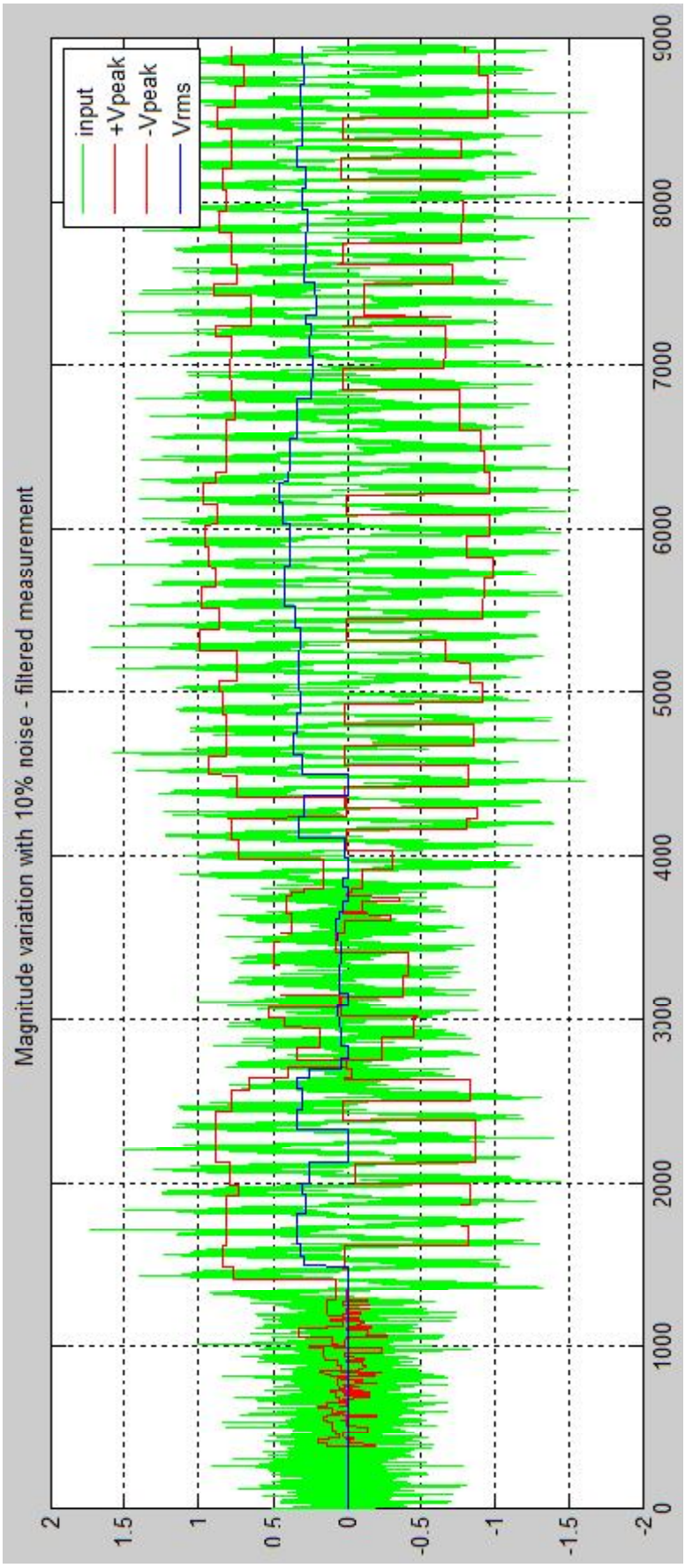
Annex 10 – Magnitude variation with noise and filtered measurement.



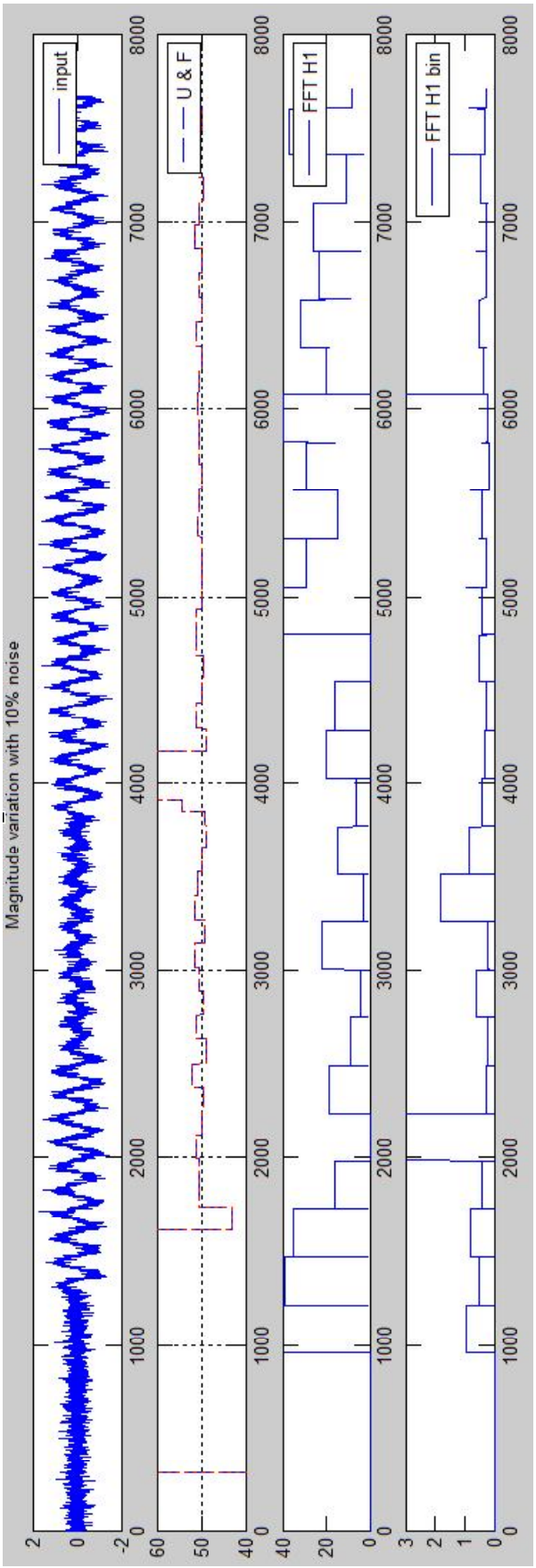
Annex 11 – Magnitude variation with noise and fundamental frequency measurement.



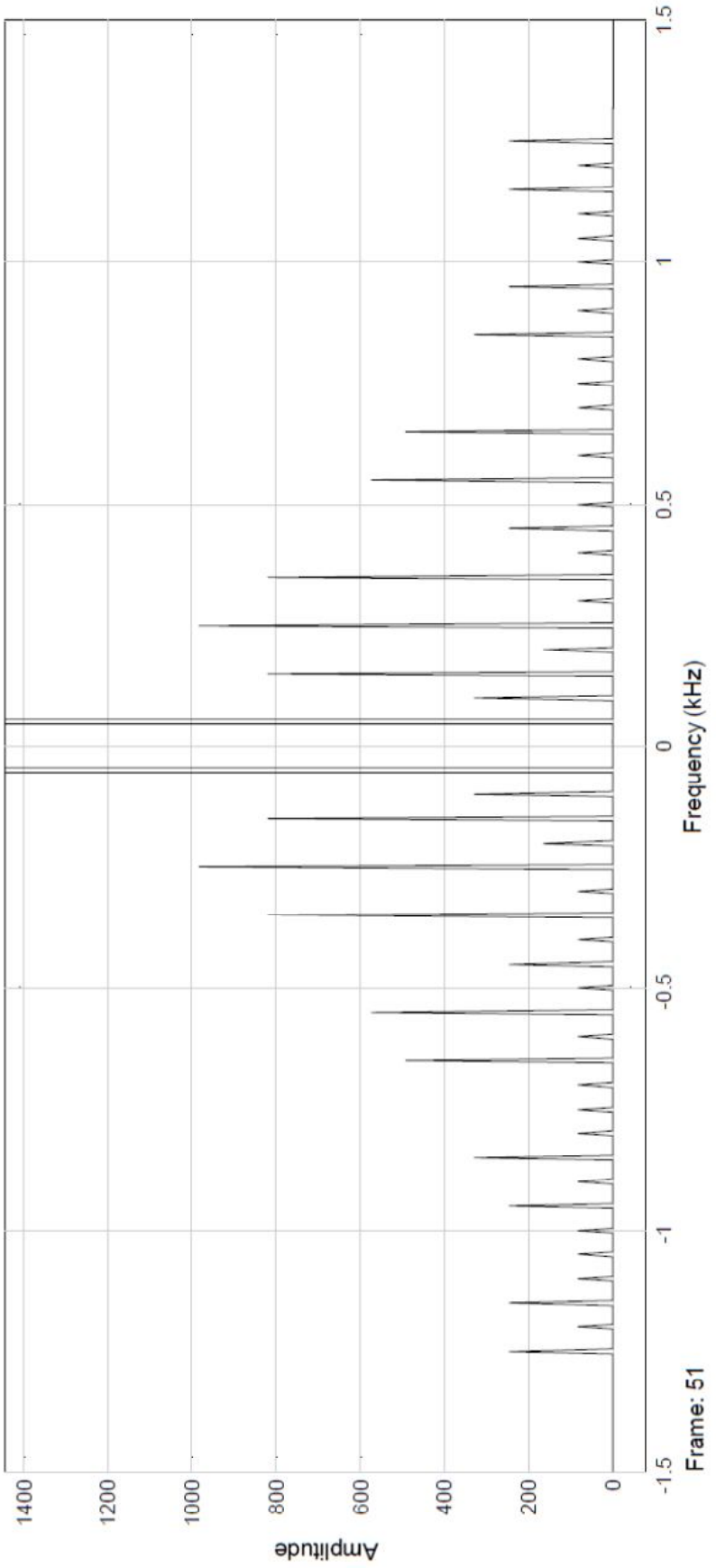
Annex 12 – Magnitude variation with noise of 10 % - unfiltered measurement.



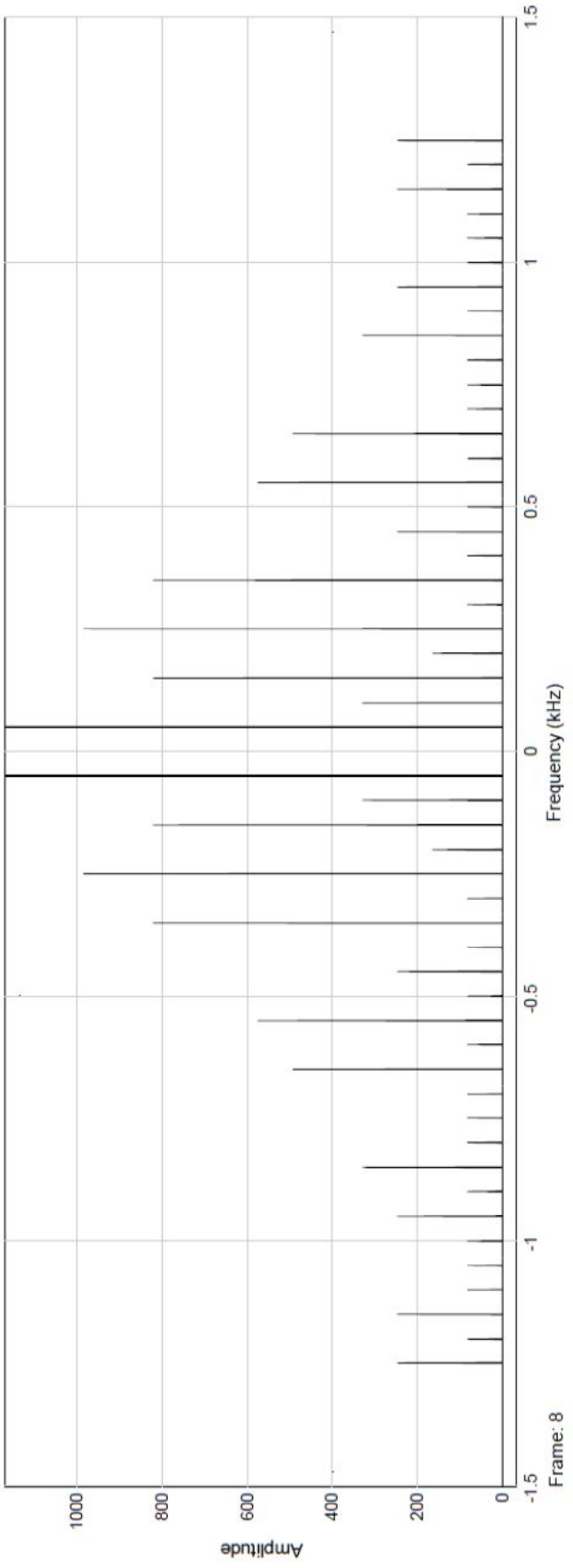
Annex 13 – Magnitude variation with noise of 10% - filtered measurement.



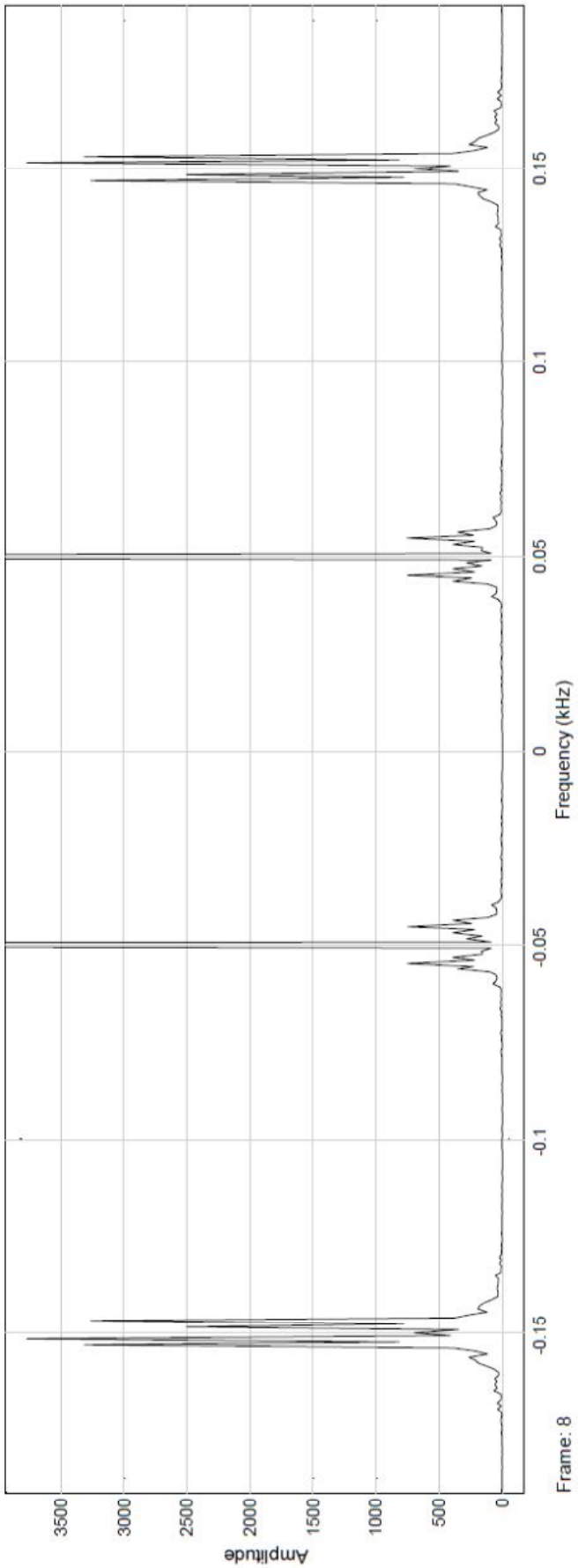
Annex 14 – Magnitude variation with 10% noise & fundamental frequency measurement.



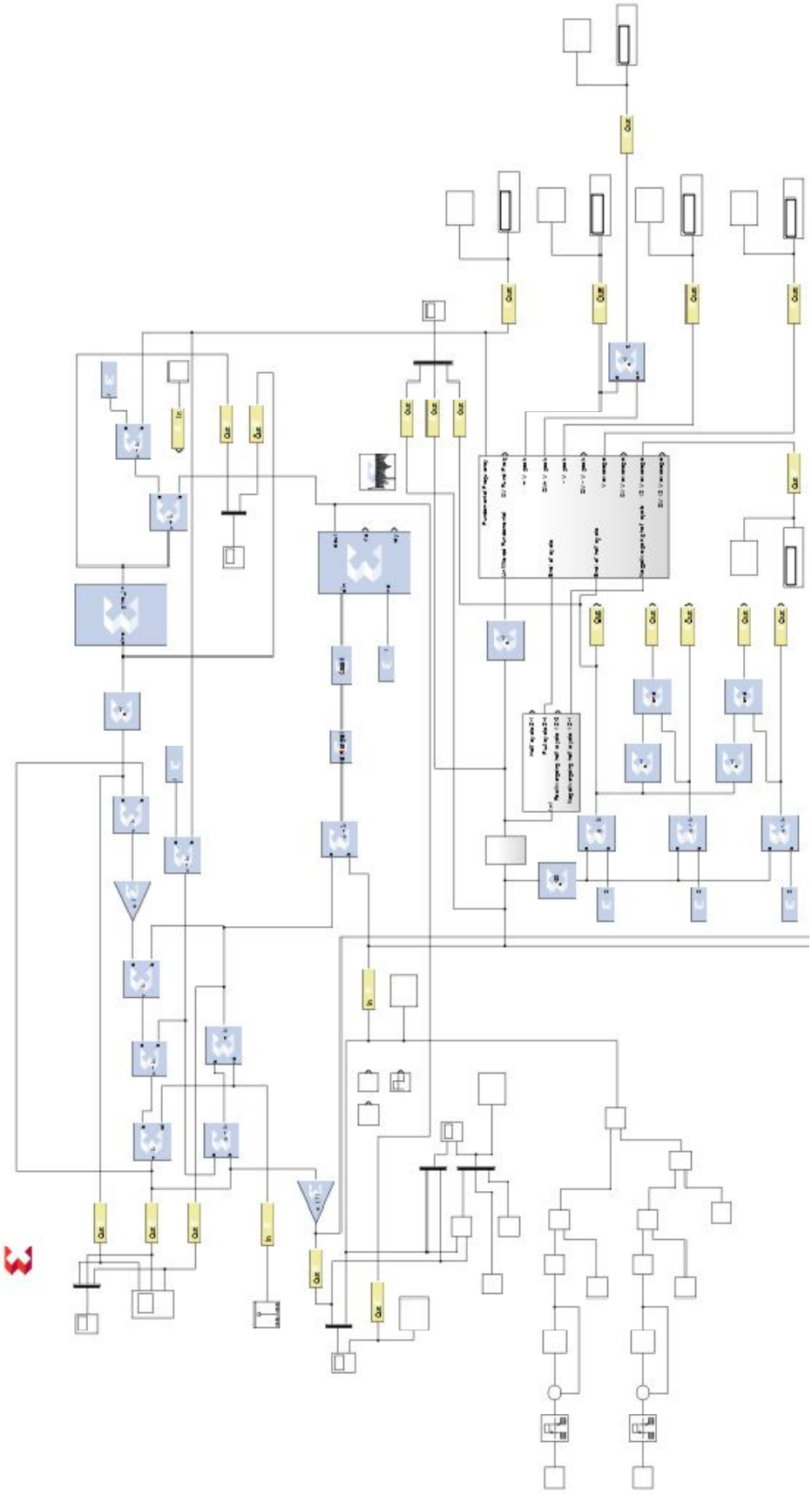
Annex 15 - Fundamental frequency of 50Hz and the first 25 harmonics with bin of 10Hz.



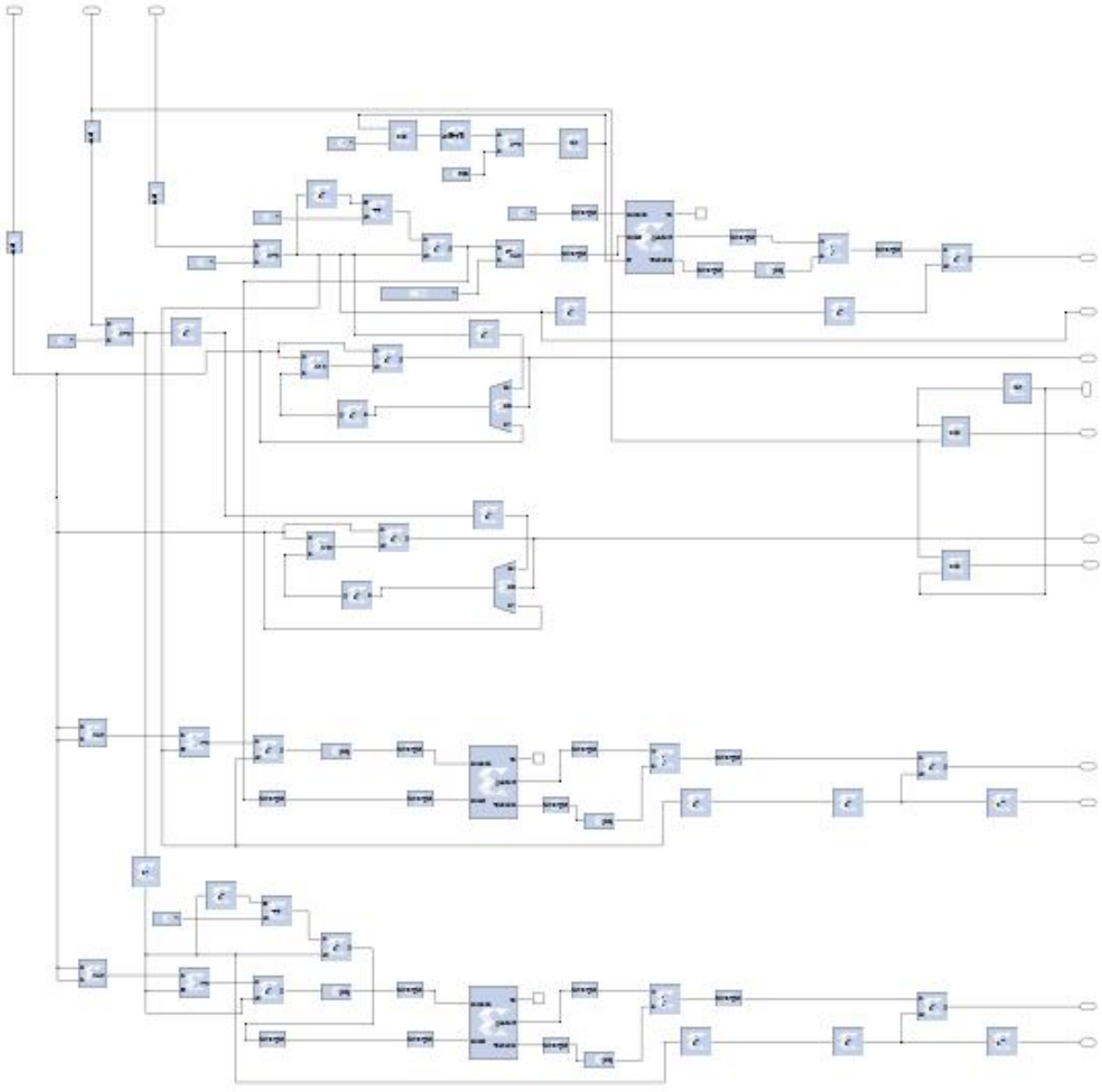
Annex 16 – Fundamental frequency of 50Hz and the first 25 harmonics with bin of 1.5Hz.



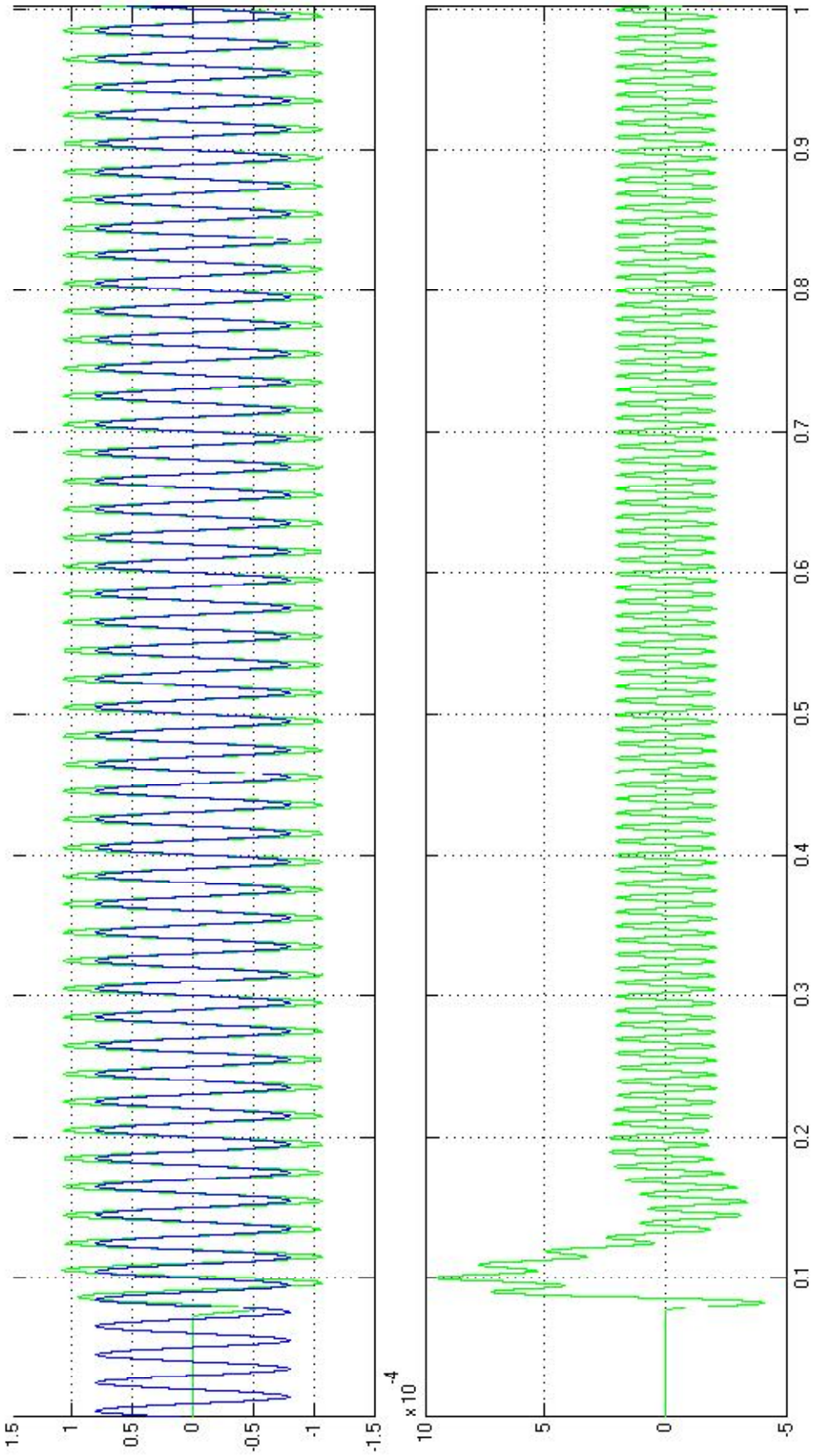
Annex 17 – Fundamental frequency at 50Hz, 147Hz, 148.5Hz, 151.5Hz and 153Hz.



Annex 18 – PLL full system.



Annex 19 – Fundamental frequency and half-wave rms measurement subsystem.



Annex 20 – Gradual adjustment of FIR filter output.

Glossary

Analyser – monitoring device that measures the input signals and classifies the phenomena detected.

Dip – a lowering of the magnitude of the input signal with recovery back to the original magnitude.

Disturbance – a situation other than normal, an exception.

Flicker – visual sensation of a fluctuation in the light intensity that can cause headaches or even provoke epileptic fits in some people.

Fundamental frequency – the frequency of the mains voltage or current expected from the electric grid.

Electric grid – the name given to the physical electrical distribution network.

Harmonic – multiple of the fundamental frequency superimposed on the input signal.

Mains signalling – communication over power lines, signals superimposed on the voltage waveform.

Swell – an increase of the magnitude of the input signal with recovery back to the original magnitude.

Transient – abrupt oscillating transition with a rapid damping decay.

Variation – any deviation from the expected signal waveform where stationary signal variation is a gradual deviation and event is an abrupt deviation.