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All-digital reconfigurable STDCC radar baseband implementation in FPGA

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***Abstract*—This paper reports the architecture of an all-digital Swept Time-Delay Cross-Correlator (STDCC) baseband. Until recently, the sliding correlator technique has been mainly employed for sounding the radio propagation channel. However, recent benchmarks have shown promising results in target detection context when compared to commercially available solutions. STDCC takes advantage of the sliding correlation properties of Pseudo-Noise (PN) sequences. Therefore, this paper presents the baseband generation for this new radar technique with on-the-fly sequence tuning using a Field-Programmable Gate Array (FPGA). The reconfigurable STDCC radar baseband generates both PN sequences digitally and requires a low-cost ADC to acquire the time dilated result. At the end, the proposed architecture is evaluated regarding resource usage efficiency and then the radar performance will be discussed in terms of the all-digital PN sequence spectrum and the real-time slide correlation. Our analysis confirmed a strong correlation between both sequence length and sampling frequency with radar detectable distance.**

***Index Terms*—RADAR, STDCC, PN sequences, FPGA.**

I. Introduction

RAdio Detection And Ranging (RADAR) has been in existence for nearly a century with an initial interest towards military applications. In the last decade, radar has been extensively studied for many other applications, but it is foreseen that, in the near-future, drone and automotive industries will massively deploy such technology. Consequently, such a continuously growing trend encourages the development of novel radar technologies with sophisticated algorithms and with new waveforms able to mitigate radar interference.

Until recently, the radar waveform commonly employed for drone and automotive sectors was called Frequency-Modulated Continuous Waveform (FMCW) [1]. Such technique transmits a continuous wave that varies the frequency with respect to time, which achieves a saw-tooth frequency modulation sweep. However, with the envisioned number of radars skyrocketing, the FMCW will soon fall victim of its own success, as radar interference will degrade the target detection capability [2].

That said, new waveforms started to be proposed in order to mitigate the multiple radar interference. There have been many proposals in the literature using noise radar waveform resorting to Pseudo-Noise (PN) sequences. Besides good interference immunity, the PN radar technology has good auto correlation properties, leading to high range resolution, but it also provides low probability of interception [3]. However, since PN

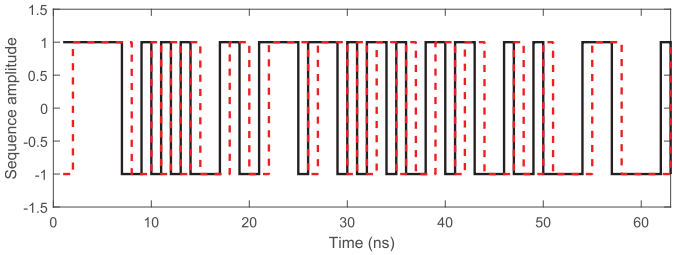

Fig. 1: Sliding correlation principle.

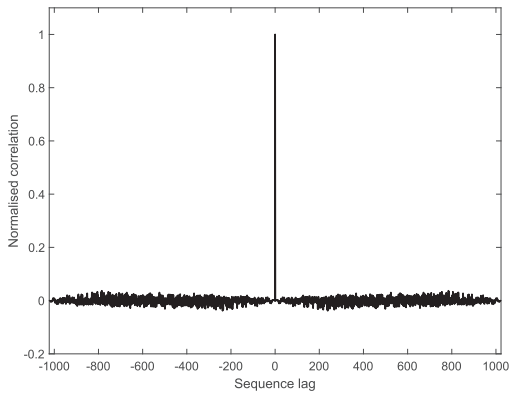

Fig. 2: Autocorrelation result for an m-sequence, m=10.

sequences are generated digitally resorting to powerful devices with DSP capabilities (FPGAs), it then requires high-speed converters to do their conversion to the analogue domain. This latter characteristic is not ideal due to the added costs associated with ADC and DAC acquisition.

The baseband radar architecture herein proposed is based on the Swept Time-Delay Cross-Correlator (STDCC) technique, which is well explained in the literature [4]–[6]. This technique uses the sliding correlation of PN sequences (Fig. 1 and 2), which were implemented without using a DAC (all-digital). In [6], such STDCC radar operating at 24 GHz is benchmarked with a commercially available of-the-shelf FMCW solution. Considering that STDCC radar performance showed promising results, it is this work ambition to propose an improved STDCC baseband architecture to tune on-the-fly the radar parameters according to user needs.

This paper is organised as follows: section II details briefly the STDCC principle. Section III describes the proposed reconfigurable STDCC baseband architecture, giving emphasis

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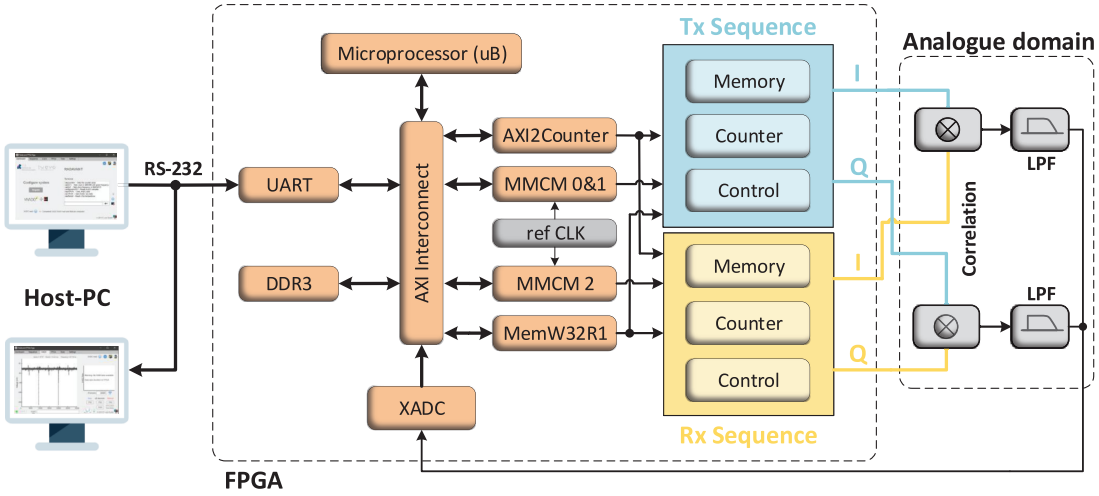


Fig. 3: Block diagram of reconfigurable STDCC radar architecture.

on the sequence generation, as well as, their sampling frequency clock generation. In section IV, the radar baseband performance is assessed in terms of resource usage, followed by the digitally generated sequence quality and culminating in their correlation results. Finally, the main conclusions are addressed in section V.

II. STDCC PRINCIPLE

As previously stated, the STDCC PN radar explores the auto-correlation properties of PN sequences. Such radar generates two identical PN sequences that are sampled at slightly different rates. As is depicted in Fig. 1, by adjusting the receiver PN sequence with a slightly slower clock, both sequences will slide with one another. When the receiver sequence (slower rate) has a perfect alignment with its counterpart, a peak value appears in the correlation output. Fig. 2 shows the correlation result, simulated in MatLab, where two PN sequences with a length of 1023 bits were correlated with the cross-correlation function. Note that the peak correlation value appears with zero sequence lag, which is when both sequences are perfectly aligned.

The sliding correlation is time dilated by a sliding factor of k, and is given by (1) [7]. The amount by which the correlation peaks are dilated is given by the transmitter PN frequency ratio with both PN sequences chip frequencies. Hence, when considering a transmitter PN sequence clocked at 500.1MHz and a receiver replica at 500MHz, we have a slide factor of 5001, therefore reducing the bandwidth requirement in the baseband data collection within the same order.

$$k = \frac{f_{seqTx}}{slip\ rate} = \frac{f_{seqTx}}{f_{seqTx} - f_{seqRx}} \tag{1}$$

According to [4], the transmitted PN places an upper bound on the radar maximum distance, proportional to the sequence length and the transmitted chirp period.

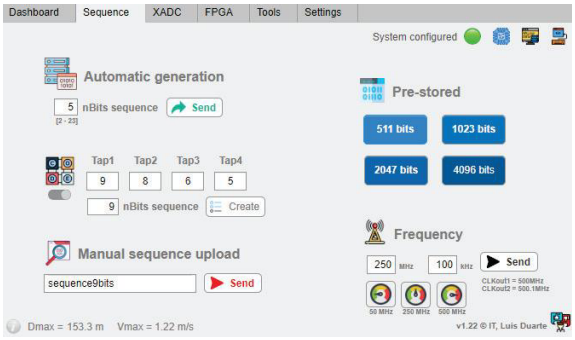


Fig. 4: MatLab app for FPGA reconfiguration.

Following this, the next chapter will discuss a reconfigurable real-time STDCC baseband capable of tuning both parameters on-the-fly.

III. RECONFIGURABLE RADAR ARCHITECTURE

The radar baseband is responsible for controlling and generating the radar signals to be transmitted, as well as linking these with those received. The proposed architecture, depicted in Fig. 3, uses a Xilinx Kintex 7 FPGA to change, on-the-fly, the utilised PN sequences and their output sampling frequency.

This architecture uses a soft-core microprocessor called microblaze (uB) responsible for routing the data inside FPGA to the required Xilinx blocks [8]. Such microprocessor receives the user parameters inserted in a MatLab GUI (Fig. 4) through a serial communication port (UART). Then, it routes the required control signals to custom made VHDL blocks called Axi2Counter and MemW32R1, which dictates the sequence length and its output sampling clock.

The all-digital sequence block design is depicted in Fig. 5 with greater detail. Such figure is a subset of Fig. 3 and it shows the control of two block memories that contain both the transmitted and receiver PN sequences.

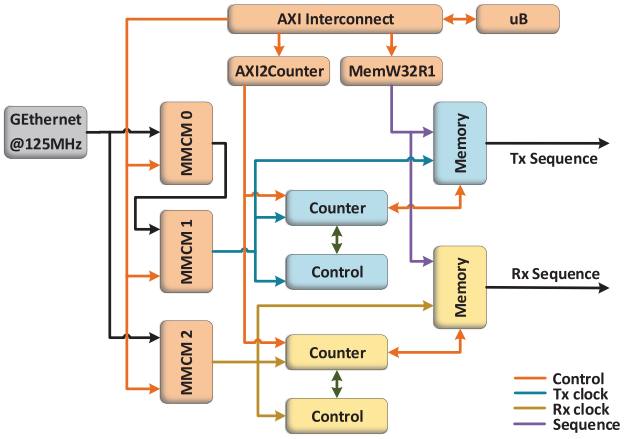


Fig. 5: Detailed overview of reconfigurable radar architecture.

Following the explained STDCC principle, the two PN sequences with a slight clock frequency offset are correlated in the analogue domain using a Mini-circuits ZFM-2-S+ mixer. The correlation mixer has a RF/LO range from 1 to 1000 MHz, necessary to output the correlation result which is in the order of few kHz. However, as stated in [4], the correlation operation performed by the mixer introduces high order intermodulation distortion (IMD). Thus, a low-pass filter is important to produce a clean time-dilated correlation product. Therefore, a 10th order low-pass filter (LPF) with a cut-off frequency at $2 \times sliprate$ was employed after the mixer and before the correlation acquisition.

In the end, a 12-bit 1 Mega sample per second ADC already present in the KC705 development board (XADC), acquires the correlation result for post-processing and plot within the same MatLab GUI.

A. Sequence generation

The proposed STDCC radar baseband uses PN sequences that are MLSR type (Maximal Length Linear Shift Register). The MLSR, also known as m-sequences, are a type of spreading sequences that present good auto-correlation properties. The m-sequence has an odd length of $N = 2^m - 1$ and a similar statistical distribution of ones and zeros (always has an extra value of one) and thus a constant power envelop.

The m-sequence generation is accomplished with a series of shift registers with feedback taps and modulo-2 adders. By varying the feedback taps according to the Table in [9], different sequences lengths are generated.

To increase the system flexibility and allow a future study of several sequence types (Gold, Kasami, Walsh, Zadoff-Chu), the sequence generation is performed in MatLab and downloaded to FPGA block memories. This work uses a 4-tap linear feedback shift register script that together with the tabular values given in [9] generates m-sequences of various lengths.

A microprocessor in FPGA (microblaze) is necessary for controlling the sequential memory write, as well as to process all the user selected STDCC parameters into FPGA native signals. Thus, the MatLab script groups the generated m-sequence into words of 32 bits to match the microblaze 32-bit architecture. Then, the MatLab app (Fig. 4) transmits them through serial communication (RS-232) to the FPGA microprocessor registers. After this, the sequence is routed via AXI protocol to the MemW32R1 custom-made VHDL IP block. Lastly, the MemW32R1 is responsible for decoding the AXI signals back into the original 32-bit sequence data while also generating the memory write address of the dual-port RAM storage.

A dual-port RAM is a memory type that allows multiple reads and writes to occur at the same time with different clock frequencies. That allows the sequence configuration to operate at microprocessor speed (memory write), while the sequence output can operate at the desired sampling frequency described in next Section (memory read).

The proposed architecture (Fig. 5) uses a reconfigurable counter to produce the read address for the dual-port RAM containing the sequence. Similar to the memory configuration, the counter control receives the sequence length value from the microblaze via a custom-made AXI2Counter block. This value will be compared against the last read address and will trigger the counter reset if memory length has been achieved. It should be noted that clock cross-domain techniques are required to intertwine the signals in the control block, since the sequence configuration operates at microprocessor clock (200 MHz) and sequence output operates at the desired sampling frequency (up to 500 MHz). In the end, we have two fully controlled dual-port RAM memories storing the two sequences that are each outputted in a KC705 SMA pin. Therefore, creating an all-digital m-sequence output with controlled sampling clock and without requiring an analogue converter board (DAC).

B. Sampling frequency algorithm

The possibility to tune the sequence output sampling frequency on-the-fly is another important characteristic envisioned for the reconfigurable STDCC baseband. By changing both the transmitter and receiver output frequencies, the user can vary the output bandwidth and the sliding factor, that, in the end, will adjust both the radar maximum detectable distance and speed.

The STDCC slip rate is usually within the hundreds of kHz, meaning that the difference between both transmitter and receiver sampling frequencies is quite small. To achieve such precise frequency values inside FPGA can be quite cumbersome using low-quality clock references. Hence, the proposed architecture uses a low-jitter 125 MHz clock chip present in the KC705 development kit, which is normally employed for gigabit ethernet (GbE) clock generation (ICS844021I) [10].

As can be seen in Fig. 5, such GEthernet clock is used by two clock generating blocks (MMCM) as input reference, that synthesise the transmitter and receiver sampling frequencies.

The Mixed-Mode Clock Manager (MMCM) are used within the Xilinx Vivado environment to implement a clocking network matched to the designer requirements. Such blocks were connected to the microprocessor via AXI bus to allow a

dynamic reconfiguration of their clocking primitives [11] and achieve the user's selected sequences sampling frequencies.

As stated in [12], each MMCM can synthesise up to 7 different frequencies with the following relationship:

$$CLK_{out_N} = CLK_{in} \times \frac{Mult}{Div \times Div_N} \ , \tag{2}$$

where N is the output number, CLK_{in} is the mentioned reference clock, $Mult$ is the MMCM fractional multiplication, Div is the MMCM integer division and Div_N the fractional multiplication for a given output clock.

Since the chosen KC705 development board has a Kintex7 FPGA with a -2 speed grade that has a VCO_{max} of 1440 MHz [13], the ideal $Mult$ value is given by:

$$Mult_{ideal} = \frac{Div_{min} \times VCOmax_{KC705}}{CLK_{in}} = 2.88 \ . \tag{3}$$

The MatLab script calculates the MMCM multiplication and division configuration parameters to best match the desired clock frequency. Considering the fractional operations step of 0.125 and respecting the given FPGA model limitations, the algorithm computes both Eqs. 4 and 5 to achieve the desired bandwidth and slip rate given its 125MHz input clock.

$$CLK_{Tx} = CLK_{in} \times \frac{Mult_{MMCM0}}{Div_{MMCM0} \times Div_{CLK0}} \times \times \frac{Mult_{MMCM1}}{Div_{MMCM1} \times Div_{CLK0}} \tag{4}$$

$$CLK_{Rx} = CLK_{in} \times \frac{Mult_{MMCM2}}{Div_{MMCM2} \times Div_{CLK0}} \tag{5}$$

It should be noted that both sampling frequencies are quite close, meaning that an architecture with a single clock generation block cannot synthesise a clock with few hundreds of kHz of precision. Thus, two MMCM (0 and 1) connected in cascade mode will operate together to fulfil the required sampling frequencies for the transmitter. For instance, to obtain the transmitter sampling frequency of 500.1 MHz, the MMCM0 outputs a clock of 33.866359 MHz that is converted to the desired 500.1 MHz by the MMCM1 (closest match of 500.100180 MHz).

With the reconfigurable architecture fully detailed, a set of performance evaluation indicators were taken that are discussed in next section.

IV. Experimental results and discussion

In this section, the proposed reconfigurable radar is assessed in terms of its resource usage efficiency. Then, the all-digitally generated sequences are evaluated according to their power spectrum and their autocorrelation properties in back-to-back (B2B) configuration mode (Figs. 6 and 7) will be discussed.

A. Hardware resources

The implementation of such architecture, besides reconfigurability, also aimed at the minimisation of hardware resource utilisation. Currently, in terms of memory usage, the design uses 4096-bit memories to allocate each sequence, while also providing space for processor data/instructions and for the temporarily XADC captured data. Despite all this, according to Table I, the Block RAM (BRAM) utilisation is still quite low ($< 7\%$), leaving room for future design increments if care is taken to keep the current timing constraints that achieve a 500 MHz output sequence.

On the other hand, in terms of clock resources for the microprocessor, DDR3, UART and reconfigurable clock architecture, 6 of the available 10 MMCMs are used. Looking at the remaining resource usage values, we can see a low utilisation of both Flip-Flops (FF) and Look up Table (LUT) of Kintex7 FPGA.

TABLE I: Reconfigurable architecture resource usage.

Resources	Utilisation	Available	Utilisation %
FF	22594	407600	5.54
LUT	24311	203800	11.93
BRAM	29.5	445	6.63
BUFG	13	32	40.62
MMCM	6	10	60.00

B. FPGA sequence output

The Agilent E4408B spectrum analyser was used to assess the all-digital sequence generation by measuring the channel power for various sequence lengths and sampling frequencies. For instance, Fig. 8 shows the frequency spectrum generated using a all-digital 9bit sequence with a sampling frequency of 500 MHz. The PN output spectrum depicted in Fig. 8 confirms the signal spectrum that follow a $\left(\frac{sin(x)}{x}\right)^2$ behaviour, with nulls occurring at multiple integers of the PN clock frequency, as expected [7].

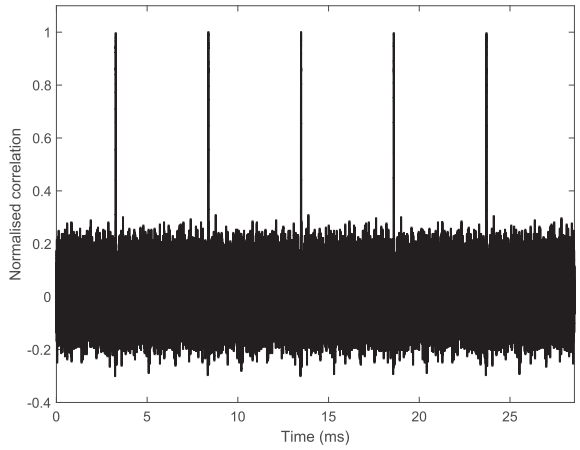
Table II summarises the measured channel power, as well as, the power at f_s and $2\times f_s$ across multiple sequences (from 9 up to 12) and different sampling frequencies ($50, 250, 500$ MHz). Table II shows that the channel power stays relatively constant around 12.89 dBm/500MHz for different sequence lengths. However, by decreasing the sequences sampling frequencies a slight performance degradation appears.

C. Back-to-back performance

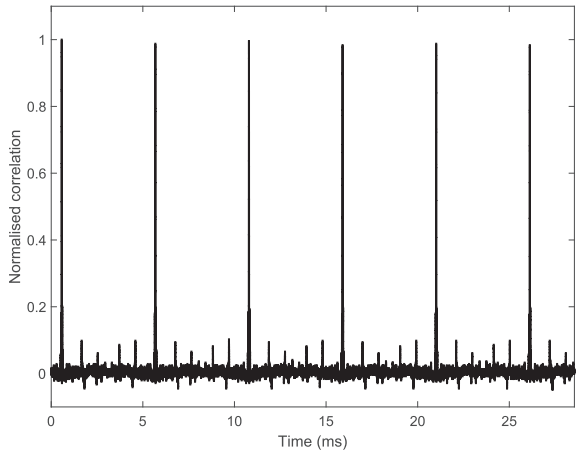
As can be seen in Fig. 9, two FPGA pins are responsible for outputting the sequences selected in MatLab App, requiring three input parameters that are the sequence length, Tx and Rx sampling frequencies. As mentioned, the Tx and Rx sequences have a slight frequency offset that performs the sliding correlation when connected to the RF and LO ports of the mixer. For simplicity purposes the result discussion will be for the I component only and with a fixed sliding factor of 100 kHz. The correlation result present at mixer's IF port

is connected to a LPF with a 200 kHz cut-off frequency and then captured by the FPGA XADC pins.

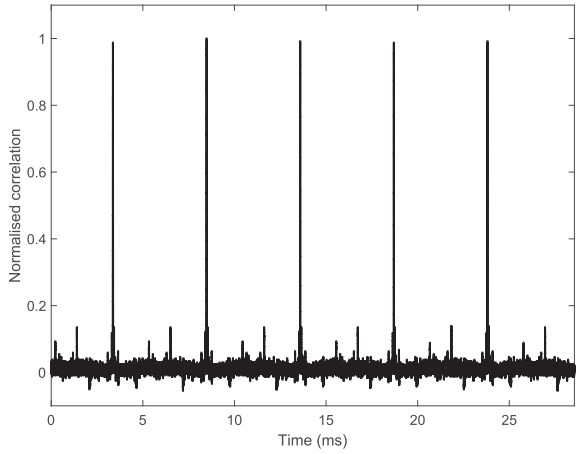
Figs. 6 and 7 show the STDCC baseband result, in B2B configuration, using a PN sequence length of 511 (m=9) and 1023 (m=10) respectively. In those figures, for each sequence length, the receiver sampling frequency was tuned to $[50, 250, 500]$ MHz that together with the fixed 100 kHz slip rate form a Tx=$[50.1, 250.1, 500.1]$ MHz. Table II compiles all the sequence lengths benchmarked with three sets of sample frequencies, showing the proposed reconfigurable STDCC radar performance (SNR).



(a)

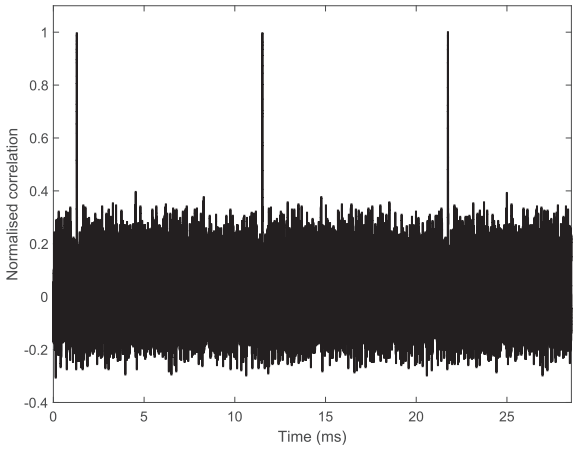


(b)

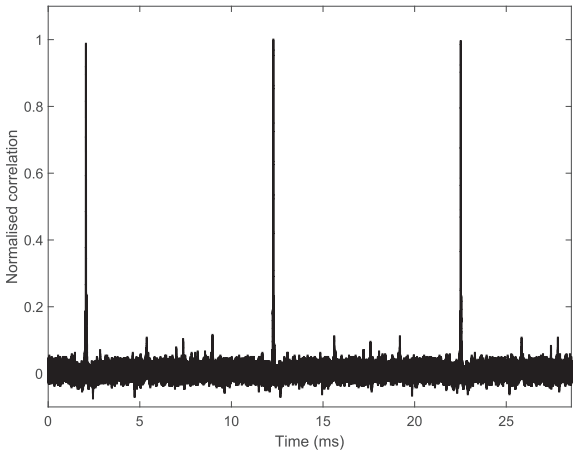


(c)

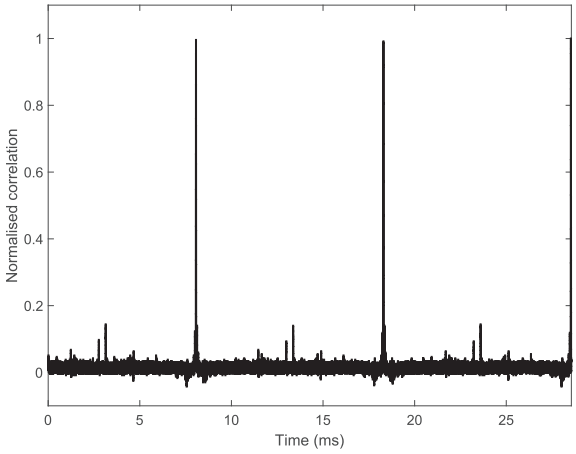
Fig. 6: Normalised captured CCF for an m-sequence, m = 9 with a) 50 b) 250 and c) 500 MHz output sampling frequency.



(a)



(b)



(c)

Fig. 7: Normalised captured CCF for an m-sequence, m = 10 with a) 50 b) 250 and c) 500 MHz output sampling frequency.

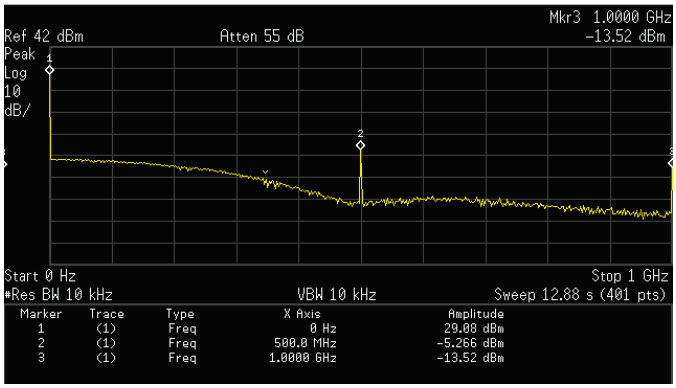


Fig. 8: Output spectrum of all-digital m=9 sequence.

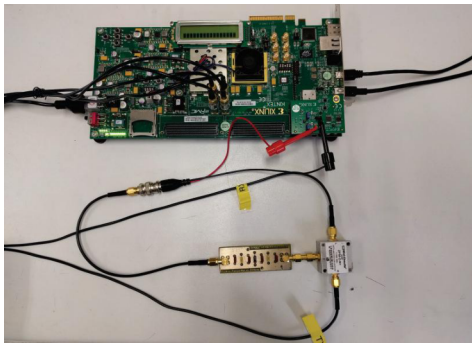


Fig. 9: KC705 FPGA with correlation and filtering.

The theoretical normalised auto-correlation result of a PN sequence, is represented by a triangular shape with apex set at value 1 and the base with a width of $N \times Tc$ set at $-1/N$ value, as can be seen in [5]. Thus, by increasing sequence length, the calculated SNR is expected to decrease since the noise floor will approximate zero value.

Looking at the measured correlation results presented in Table II, a strong relation between f_s/L and the SNR was observed, thus being closely associated with radar maximum detectable distance. It is shown that the normalised correlation peak to noise ratio (SNR) decreases with higher length sequences and lower output sampling frequencies (Table II), as expected.

TABLE II: Summary of the power measurements and SNR for various m-sequence lengths and sampling frequencies.

Measurement [dBm]	**Sequence (bits)**	**Sample frequency (f_s)**		
		50 MHz	**250 MHz**	**500 MHz**
Power @ f_s [dBm]	9	-24.68	-10.30	-6.48
	10	-24.71	-10.34	-6.59
	11	-24.75	-10.37	-6.62
	12	-24.82	-10.37	-6.67
Power @ $2 \times f_s$ [dBm]	9	-24.90	-13.28	-15.19
	10	-24.93	-13.32	-15.23
	11	-24.97	-13.35	-15.26
	12	-24.97	-13.35	-15.30
Channel Power [dBm/f_s]	9	13.45	13.17	12.89
	10	13.41	13.18	12.87
	11	13.40	13.15	12.85
	12	13.40	13.13	12.82
Normalised correlation peak to noise ratio (SNR)	9	0.531	0.794	0.834
	10	0.469	0.727	0.821
	11	0.457	0.723	0.816
	12	0.413	0.678	0.783

V. Conclusions

This paper presented a reconfigurable architecture suitable for STDCC performance evaluation. The proposed architecture allows a on-the-fly sequence length tuning together with output sampling frequency adjustment. It has shown benefits with its all-digital architecture that does not require a DAC usage, and with its sliding correlation principle that requires a low-cost ADC acquisition board (XADC). Finally, this work shows a strong dependency between STDCC parameters and the radar detection performance. As expected, with shorter sequences and higher sequence sampling frequencies, the normalised correlation peak to noise ratio is increased, thus improving the radar maximum detectable distance.

Acknowledgment

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