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Multi-Gigabit/s OFDM real-time based transceiver engine for emerging 5G MIMO systems

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ABSTRACT

This paper presents a highly scalable multi-Gigabit/s Real-Time (RT) Wideband (WB) Orthogonal Frequency Division Multiplexing (OFDM) processing chain for 5G applications. It is aimed to significantly reduce the Hardware (HW) footprint of Multiple Input Multiple Output (MIMO) systems. In this context, implementation complexity results for MIMO configurations of 2 × 2, 4 × 4 and 8 × 8, enabled at sampling rates of 245.76, 122.88, 61.44 and 30.72 MHz, respectively, are compared with the ones from conventional MIMO architectures. For example, for a 8 × 8 MIMO–OFDM configuration implementation, savings of up to 87% are achieved when compared with conventional design methods, in terms of DSP48E1 slices. Moreover, in a *Xilinx* Virtex 7 XC7VX485T, it is shown that a second processing branch might be implemented, leading to a 5 Gbps (using 1024 Quadrature Amplitude Modulation (QAM)) Single-Input Single-Output (SISO) link or a 16 × 16 MIMO configuration. Finally, in order to validate the proposed architecture, the impact of its inclusion on a complete Field Programmable Gate Array (FPGA) 8 × 8 OFDM system, at LTE's highest sampling rate of 30.72 MHz, is evaluated. Subsequently, it is demonstrated that this does not affect the performance of OFDM, even in the presence of Carrier Frequency Offset (CFO).

1. Introduction

Providing solutions for the expected explosive growth of mobile data users, and subsequently massive data traffic to be accommodated by mobile networks, is currently a subject of great interest within the wireless scientific community. In this context, official standardisation bodies such as 3GPP are developing the first set of 5G standards, aiming to interconnect a massive number of users and devices [1,2]. Specifications for the 5G New Radio (NR) has been recently made available in [3,4]. In this context, NR is based on Orthogonal Frequency Division Multiplexing (OFDM) modulation, with an optional feature of using a discrete Fourier transform (DFT) precoding to boost the power amplifier efficiency. Moreover, NR flexibility allows the support of multiple sub-carrier spacings, ranging from 15 to 240 kHz, depending on the deployment scenario and application. For example, according to [3,5], 15, 30, 60 kHz are the sub-carrier spacing for the sub-6 GHz systems with a maximum signal Bandwidth (B) of 200 MHz, whereas, 60, and 120 kHz are established for the mmWave communications. Furthermore, it is expected that massive Multiple Input Multiple Output (MIMO) antenna configuration systems [3], which employs hundreds of antenna elements [6], will be deployed along with the NR described above. Such system deployment will compensate for large propagation path loss and achieve very high bandwidth efficiency with the aid of multibeam multiplexing transmission capability [7,8], where data is transmitted simultaneously to several users (MU-OFDM).

To this extent, working on the development of technology capable of providing such applications, is both timely and topical. The availability of new rapid design, validation flows and related real-time prototyping experiments are of significant interest for performance validation and proof-of-concept of the various proposed communication techniques. In this context, multi-Gigabit/s data transmission, and Hardware (HW) efficiency are seen as the most relevant Key Performance Indicator (KPI) metrics for future mobile terminals and networks [9–12], in particular at mmWave frequencies [13].

A number of articles addressing data rates of multi-Gigabit/s are already available in the scientific literature. However, none of them are Real-Time (RT) based prototypes. For example, in [14], authors achieve 10 Gbps, but the transmitted data is initially stored in a dedicated Field Programmable Gate Array (FPGA)

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memory and played back in loop. At the receiver, samples that are acquired by an Analogue-to-Digital Converter (ADC) are stored in another memory for subsequent post-processing. Moreover, despite of the existence of a few articles describing architectures, implementations and platforms that offer the possibility to implement and test algorithms for MIMO–OFDM-based systems, to the authors' knowledge, none of them present a signal processing efficiency close to the one proposed in this work. For example, in [15], for a 2 × 2 MIMO antenna configuration, the input data stream is multiplexed in two parallel Single-Input Single-Output (SISO) paths, doubling the system complexity when compared with SISO. Similarly, in [16–18] the same concept is adopted, where one pair of Inverse Fast Fourier Transform (IFFT)/Fast Fourier Transform (FFT) is used for each MIMO Transceiver (TRX) path. In [19,20], although a 128 × 8 MIMO antenna configuration is considered, only the receiver detector is implemented in hardware. The real-time SISO LTE platform presented in [21], is limited to 20 MHz of signal Bandwidth, which leads to a very limited potential to process post-4G Ultra Wideband (UWB) systems. Finally, in the prototype Massive MIMO testbed reported in [22,23], HW efficiency seems to be an issue, since each *Xilinx* Kintex-7 FPGA processes a single antenna path, resulting in a bulky and power consuming system.

Unlike the state of art, this paper proposes a high-performance OFDM TRX engine for the prototyping of advanced 5G communications systems, capable of achieving multi-Gigabit/s RT transmission. Moreover, it also addresses the design of various MIMO configurations exploring the single OFDM processing path. Experimental results show that a single TRX path implemented in a *Xilinx* Virtex 7 FPGA, running at 250 MHz, enables an aggregated bandwidth higher than 246 MHz, achieving data-rates over 2 Gbps, with a processing load over twenty Giga Multiply-Accumulate operations per Second (GMACS). The structured design approach enables a single TRX OFDM modulator engine to process data for different antenna configurations at the expense of system's bandwidth, i.e., it supports a 8 × 8 MIMO antenna configuration utilising a single pair of IFFT/FFT processing blocks, targeting LTE's maximum sample rate of 30.72 MHz. This feature significantly reduces the hardware footprint needed to implement MIMO systems, by reusing the processing potential of the TRX. This work is a major evolution from [24], where the fully pipelined hardware architecture was used to implement an over-the-air OFDM SISO transceiver, achieving a maximum baseband bandwidth of 61.44 MHz.

Finally, a 8 × 8 MIMO FPGA hardware implementation will be used to demonstrate that the proposed MIMO–OFDM modulation/demodulation architecture does not induce any degradation in terms of OFDM performance over an Additive White Gaussian Noise (AWGN) channel and in the presence of Carrier Frequency Offset (CFO). For this purpose, two metrics are considered, namely Error Vector Magnitude (EVM), also known as Received Constellation Error (RCE), and Bit Error Rate (BER).

This paper is organised as follows: Section 2 introduces the proposed Modular Architecture for Wireless Prototyping (MAWP). Section 3 presents the proposed hardware design for MIMO–OFDM systems based on the LTE downlink physical layer. Its characterisation in terms of both processing and logical resource usage efficiency is also given in comparison with conventional designs. Hardware system performance results followed by a critical discussion are presented in Section 4. Finally, the main conclusions are drawn in Section 5.

2. Modular architecture for wireless prototyping - Overview

The suitable choice of the implementation architecture and system-level design flow (and associated tools) may dictate the success or failure of the platform. Statistics shows that 60%–70% of the entire product cycle for a complex logic system is targeted to verification tasks [25]. System level development flows, like the ones proposed by *Matlab's Simulink* together with *Xilinx's* SysGen can lead to the design of a synchronous multirate system, resorting to clock enabling. This clocking architecture enables a faster development and simpler verification of the system with the provided debugging tools. Design and verification need not to be concerned with pipelining or registering. However, the simpler clocking structure hides longer critical paths that limit the system's maximum clock frequency (therefore leading to sub-optimal performance), and the need to distribute a low-skew clock to the entire design, with significantly more demanding clock driving and associated power consumption. In this context, the MAWP considered in this work is based on the one proposed in [24], where it has been demonstrated that its utilisation successfully reduces the length of clock paths, leading to increased overall performance/throughput of the system, by pushing the system's maximum clock rate. The decoupling of the processing in each block, leads to different processing duty-cycles for the different blocks, opening way to the use of energy efficient techniques (like clock gating) to reduce the system's overall power consumption.

The adopted architecture allows the designer to reduce the time to market requirements from the system design to its deployment, due to the ability of the user to validate each processing block individually and independently from the full digital processing chain. Also, the use of interfacing First-In First-Out (FIFO) memories constrains the clock signal path to small synchronous islands, and thus, inter-block strict timing synchronisation requirements are relaxed. The modular architecture of MAWP is the key feature that sets it apart from other hardware architectures. The digital signal processing templates for transmitter and receiver are presented in Fig. 1, and as can be seen from the figure, each one has independent processing (*proc.*) and control (*proc. CTL*) elements, resulting in a fully decentralised architecture with parallel processing. The template for both sides is similar. The difference resides in the organisation of the individual elements in the blocks, imposed by the presence of analogue-to-digital interfaces.

The DSP algorithm is implemented in the *Proc.* block. The processing is under the control of a Finite State Machine (FSM) present in the *proc. CTL* element. A FIFO buffer element, *Buffer-FIFO*, is the block responsible to interface adjacent processing blocks and provides the fill level indication signal, to the buffer level monitoring element *BufCTL*. Each processing block implements a soft handshake with the neighbouring blocks to control the generation/consumption of processed data.

3. Hardware design method for MIMO–OFDM systems

MIMO is envisaged to be one of the key technology to be adopted in future 5G wireless communications systems [26]. For example, exploiting the spatial multiplexing of the antennas at both Transmitter (TX)/Receiver (RX) ends, spectral efficiency and data rates are significantly boosted when compared to SISO systems. However, in conventional MIMO implementations, hardware complexity linearly increases with the number of used antennas. This might lead to enormous amounts of digital processing resources and energy consumption, in particular, when the number of antennas in the MIMO configuration tends to hundreds [27]. In order to overcome the hardware constraints associated with MIMO implementations, a novel MIMO–OFDM hardware architecture design is suggested to attain significant HW resource savings. The proposed architecture, depicted in Fig. 2, is composed of a single OFDM processing engine present

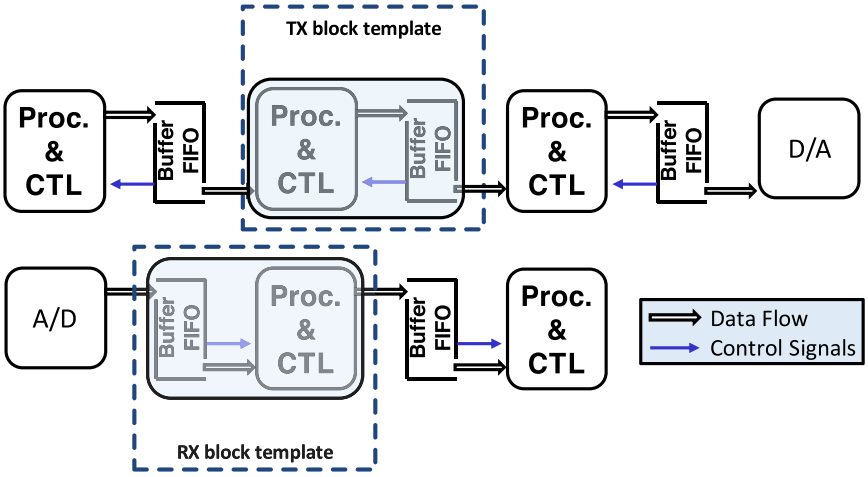


Fig. 1. Conceptual transmitter (top) and receiver (bottom) chains. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)
Source: Adapted from [24].

at both TX/RX which modulate and demodulate data symbols, from l independent antenna streams, respectively. Therefore, an interface block between *OFDM modulator and OFDM demodulator* engines and multi-processing data sources such as MIMO pre-coding, and MIMO decoder along and/or MIMO post-coding (green blocks in Fig. 2), is required. Such would allow, for example, the implementation of analogue-digital (hybrid) beamforming techniques in massive MIMO configurations, in order to mitigate user interference in ultra-dense 5G scenarios [28], while saving significant amount of logical resources. For instance, the developed architecture can also be implemented in conjunction with advanced space–time multiple-antenna codes (STBCs), such as the ones reported in [29]. In this work, it has been demonstrated that performance of space–time turbo coded MIMO systems can be significantly improved by the consideration of *Welch* constructed *Costas* permutation, which a promising MIMO coding technique to be adopted by 5G systems [30].

Since the scope of this work is to enable an hardware efficient OFDM modulation/demodulation scheme, no additional details are provided regarding MIMO pre-coding/decoder algorithms. Such is achieved through the use of multiplexing and demultiplexing entities to convert low speed parallel to high speed serial streaming data, which enables data to be processed by a single processing path. In addition, to ensure that the MIMO information is transmitted at the same rate as data is being generated, both *OFDM modulator* and *OFDM demodulator* entities have to operate at a rate greater than l times higher than the rate of both MIMO pre-coding/decoding blocks, where l is the number of antennas at both ends. With this, multiple antenna configurations are enabled by re-using the main functional DSP blocks from a typical single OFDM TRX chain. This enables higher number of paths to be processed, when compared with conventional MIMO–OFDM FPGA designs [15–18], with a reduced increment of the HW resources and footprint of the target circuit. To demonstrate this, a study on the hardware resource usage, for 2×2, 4×4 and 8×8 MIMO–OFDM configurations, employing both conventional and proposed hardware architecture designs, is conducted.

Designs are implemented in a *Xilinx* VC707 FPGA development board. It is worth mentioning that FPGA IC platform technology is the preferable choice for prototyping stages, since it ensures lower time-to-market and costs when compared to an Application-Specific Integrated Circuit (ASIC) [31]. In summary, FPGA platforms bring three main benefits for the designer, such as: no layout for manufacturing needed, simpler design (the software handles much of the routing, placement, and timing), and field re-programmability (a new bitstream can be uploaded remotely) [32].

Furthermore, the proposed architecture might be used in the design of massive MIMO–OFDM systems. The consideration of N parallel MIMO–OFDM TX/RX engines would enable the necessary processing power for M antenna paths, by considering $N = \lfloor M/l \rfloor$, where each MIMO–OFDM TX/RX engines process l streams. According to [33], this feature will be one of the enabling key technologies to attain the 5G requirements (5G technology is expected to provide broadband services up to 20 Gbps per cell (at least 0.1 Gbps per user) [34]. In addition, with the employment of hundreds of individual antennas, MIMO can bring to the 5G network benefits such as: diversity, spatial multiplexing, multiple access and beam-forming [33]. While the first enables the transmission of multiple copies of the same data over independent multi-path channels, improving the overall reliability of the wireless communication, spatial multiplexing increases the capacity of the network by transmitting different signals over each antenna path [33].

Finally, traditional access schemes namely: Time Division Duplex (TDD) and Frequency Division Duplex (FDD) [35], or even the more sophisticated ones, e.g. Non-Orthogonal Multiple Access (NOMA) [36], can be also adopted in the proposed MIMO architecture. Due its modulator approach, new post coding/decoding algorithms are easily integrated with both TX/RX MIMO–OFDM engines.

3.1. Detailed description of the MIMO–OFDM architecture

Integration of new transmission schemes, air-interfaces, MIMO coders/decoders in the proposed MIMO–OFDM architecture is straightforward, as illustrated in Fig. 2. For example, from this figure, a MIMO coder can be directly connected to our OFDM modulator, which processes and modulates the pre-coder output data for each antenna path, and delivers the samples to be transmitted to all antennas simultaneously. However, this work intends to demonstrate that MIMO systems can be deployed using much less hardware resources than the ones found in literature [15–18]. In this context, the complete TRX MIMO–OFDM system of Fig. 3 was considered, without using any particular MIMO/beamforming coder/decoder algorithms. This is, green blocks highlighted in the aforementioned figure will be only considered for the study present in Section 4. In such, the l independent SISO coders/decoders were adopted to demonstrate that the proposed MIMO–OFDM architecture does not induce any

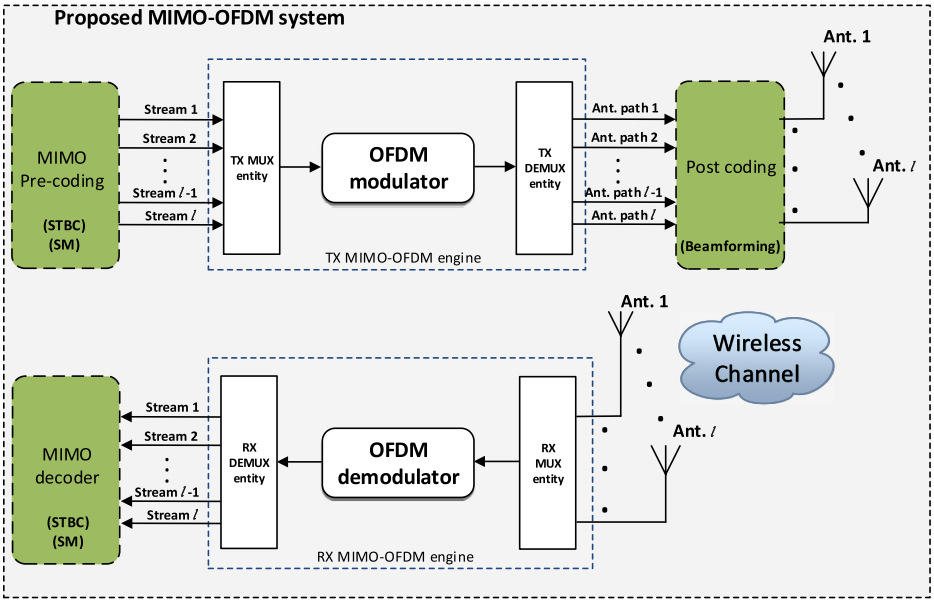


Fig. 2. Block diagram of the proposed architecture in a MIMO–OFDM system. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

degradation in terms of OFDM performance. They generate individual antenna streaming data for configurations up to 8 antenna paths. This entity is composed of a bank of parallel random binary generators together with Quadrature Amplitude Modulation (QAM) modulators and pilot sub-carrier assignment algorithms. Following this, its output data is connected to the *TX MUX* entity, which performs a Serial-to-Parallel (S/P) path conversion and selects the correct antenna path to be processed by the *OFDM modulator* DSP block (controlled by the antenna selector control signal). This entity, unlike conventional MIMO architectures, is not replicated for each antenna processing path. It performs the OFDM modulation (IFFT transform operation, Cyclic Prefix (CP) insertion) and the appending of a PHY preamble on the transmitted OFDM frame, for multiple antenna paths. Next, its output data is connected to the *TX DEMUX* block, which performs the opposite operation of the *TX MUX* block. Along with memory banks and processing control FSMs, it converts serial OFDM streaming data into parallel paths, and assigns them to their respective antenna path ensuring the synchronicity of the transmission. Each antenna TX path is directly connected to the corresponding RX antenna path (as depicted in Fig. 3), since the MIMO pre-coding and decoding are beyond the scope of this work. At the receiver, the counterpart of this process is implemented. Prior to the OFDM demodulator, which is responsible to mitigate CFO, to perform FFT, and CP removal, a joint timing synchronisation and CFO estimation is considered, following the algorithm reported in [37]. The blocks implemented in the MIMO–OFDM TX/RX engines perform all the processing required for over-the-air transmission. Finally, the OFDM demodulator entity performs the operations needed to recover the transmitted bits in each SISO path (deframing, channel estimation, equalisation and demapping).

The key features of the proposed architecture, and what sets it apart from the conventional method, are the consideration of *MUX/DEMUX* entities, and the implementation of high performance OFDM TX/RX engines in the MIMO–OFDM design. For example, only one IFFT/FFT pair is enough to process multiple MIMO antenna configurations. For the hardware design of such algorithms, the MAWP concept, presented in Section 2, was considered and significantly enhanced to meet the new performance requirements. Detailed hardware design of both *TX MUX* and *TX DEMUX* blocks are illustrated in Figs. 4a, and 4b, respectively. From the top figure, it can be verified that a P/S path conversion is accomplished by the use of a main FSM unit (*Proc.* element), two primitive multiplexers, one counter and two FIFOs (one for each I/Q source path). The processing control unit operates as follow: depending on the chosen MIMO configuration, it selects sequentially which sources are read from the *MIMO modulator* and how many samples are written to the interface memories. Hence, there is a read enable bit for each individual data source, namely, *Re_out_i*, where *i* is the antenna index. In the reading process of the first source path, *Re_out*_0 is set to '1' and the remaining are set to '0'. This is, it enables the data processing (read) coming from the *i*th data source path. After the required number of samples needed for an OFDM frame are reached (set in the counter limit value), *Re_out*_0 is set to 0 and *Re_out*_1 is set to '1'. This means that data source from the second antenna path starts to be read, and it stops when a frame is reached. This process is repeated for all paths. Moreover, due to the consideration of a modular and pipelined HW architecture, in order to ensure data integrity among processor elements, FIFOs memories must not operate in underflow condition. In this context, MUX Almost Empty (AE) signal is used to perform flow control and avoid FIFO underflow conditions. AE signals the consumer blocks that it must stop processing samples from the interfacing FIFOS in the next few clock cycles. Finally, after the information from last source path is processed, the first antenna is read once again. This reading loop only stops if either interface FIFOs are either empty or full, which are monitored by the other *TX Buffer CTRL* FSM. In this event, both counter and FIFO writing enabling bits (*en* and *We_data*), respectively, are set to '0'. Otherwise, these bits are set to '1'.

Similar algorithm implementation was done for the *TX DEMUX* block. A main FSM unit *Path sel.* is also responsible to control and decide when the individual FIFO's write enable bits (we_i) are asserted, while output data, namely *Data_i_I_in*, and *Data_i_Q_in*, are being read simultaneously from all memories and assigned to their respective *i* TX antenna. The number of FIFOs at the *DEMUX* entity can be adjusted depending on the considered MIMO configuration. For example, in a 2×2 MIMO system, only 2 FIFOs are used per I/Q paths. In both figures, blue lines indicate the input data buses coming from the adjacent DSP block in the architecture, dark lines represent the internal bus

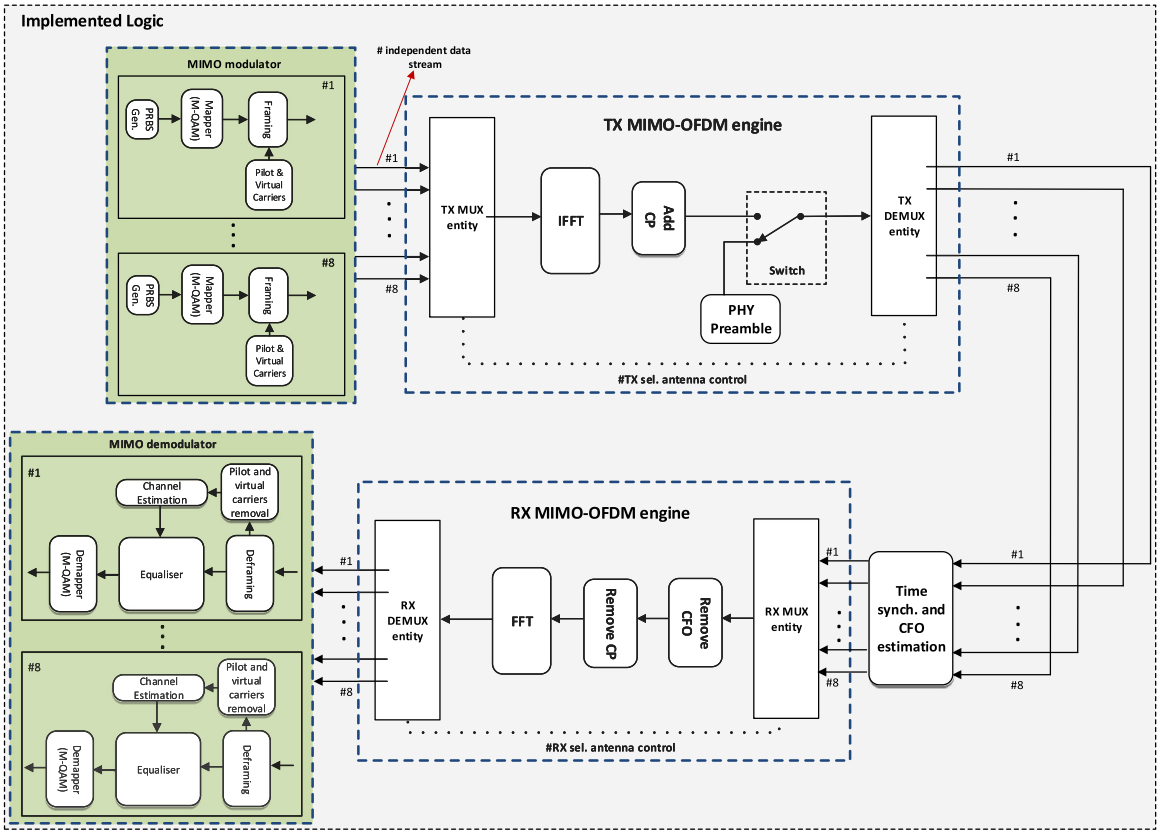


Fig. 3. Block diagram of the implemented MIMO–OFDM based engine for multiple antenna configurations. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

Table 1
Main parameters considered in the design of OFDM waveform, based on the LTE standard [38].

Parameter	Value
FFT/IFFT size block	1024
Data block size	800
Sub-carrier bandwidth	240/120/60/30 kHz
Modulation	16-/64-/256-/1024-QAM
Guard time interval	256 samples
MIMO config.	SISO/2 × 2/4 × 4/8 × 8
Sample rates per path	245.76/122.8/61.44/30.72 MHz
Maximum aggregate data rate	2.46 Gbps
Frame sample length	6400

connections in the algorithm and green ones the output data buses. In particularly, *ANT*[2 : 0] bus sets the MIMO configuration chosen by the user, i.e., when it has values equal to 0, 2, 4, and 8, SISO, 2 × 2, 4 × 4, and 8 × 8 system arrangements are selected, respectively. Finally, *RX MUX* and *RX DEMUX* were implemented just as the TX ones by adjusting the interface FIFO placement arrangement, following the template presented in Fig. 1.

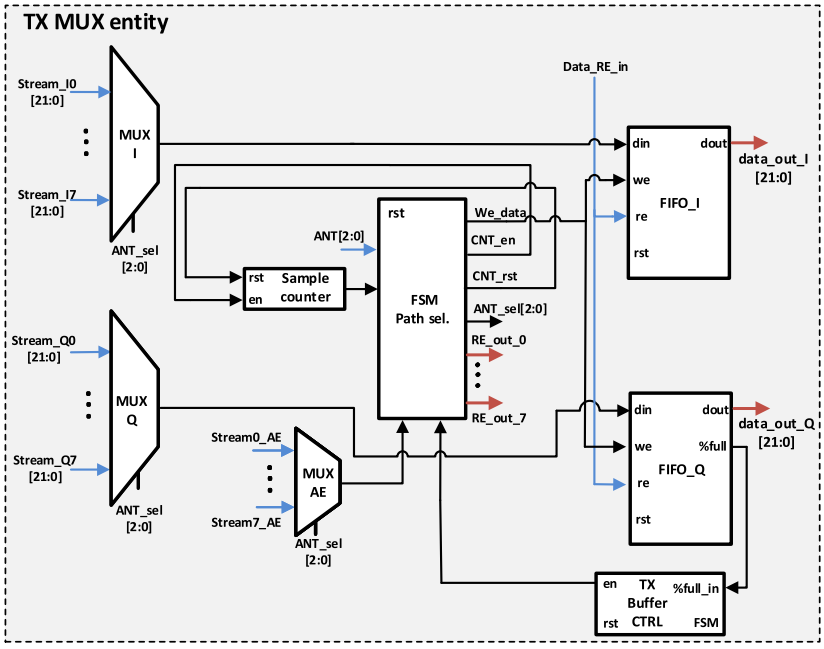
The considered OFDM waveform design parameters based on the LTE downlink Physical (PHY) layer [38], with the operating parameters given in Table 1, for 4-, 16-, 64-, 256- and 1024-QAM for 1 × 1/2 × 2/4 × 4/8 × 8 MIMO antenna configurations, which is in line with the 5G NR specifications reported in [3,5]. Here, FFT/IFFT size block denotes the total number of samples of the input discrete time-domain sequence at their input, i.e., the number of OFDM samples per symbol. In addition, frame sample length is the total number of OFDM modulated samples between two consecutive PHY preambles, which corresponds in fact, to five OFDM symbols with CP.

3.2. Hardware implementation efficiency: conventional vs. proposed method

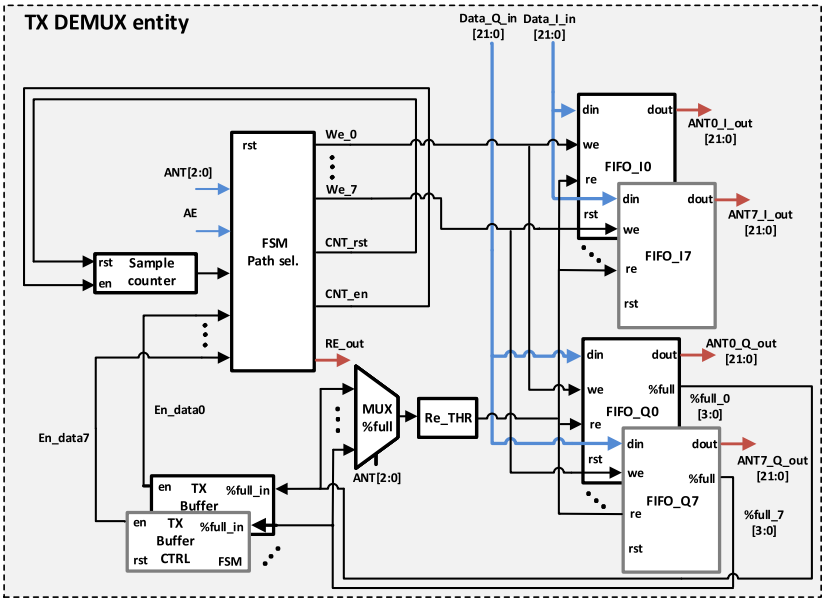
3.2.1. Used logical resources and hardware power consumption

The white blocks which compose the MIMO–OFDM transceiver illustrated in Fig. 3, were implemented in a *Xilinx* Virtex7 XC7VX485T considering both conventional and proposed MIMO–OFDM design methods, for SISO, 2 × 2, 4 × 4, and 8 × 8 antenna configurations. Following this, the amount of used logic resources was analysed in terms of the number of slices, Look-Up Tables (LUTs), Flip-Flops (FFs), DSP48E1 elements, and 36k bits Block RAMs (BRAM36k). A slice in the VC707 corresponds to 4 LUTs, 8 FFs, multiplexers and carry logic. Partially occupied slices are also included in the implementation report. Therefore, slice number is not a very accurate figure of merit for resource utilisation. However, it can be used to evaluated if mapping, routing and timing constraints of the hardware design are easily met. The hardware efficiency inherent from the utilisation of the proposed MIMO system is characterised by the amount of saved DSP48E1 slices, BRAM36k, LUTs and FFs, when compared against conventional MIMO systems. From Fig. 5a, it can be verified that the amount of saved DSP48E1s and FFs resource blocks go up to 87% and 83%, respectively, in a 8 × 8 configuration. In fact, DSP48E1 slice is the HW primitive which leads to a major contribution to the overall chip dimension. Additionally, when DSP48E1 slices, LUTS, and FFs are converted to logic gates, the total amount of saved gates is 86%, for this MIMO arrangement, as indicated in Fig. 5b. It should be mentioned that such results were obtained considering that 1 DSP48E1 slice occupies 456 LUTs and 139 FFs in the VC707, and 1 FF and 1 LUT are equivalent to 7 and 8 logic gates, respectively.

The graphical illustration of the implemented logic area (subjective analysis) in the VC707 using the proposed MIMO method



(a)



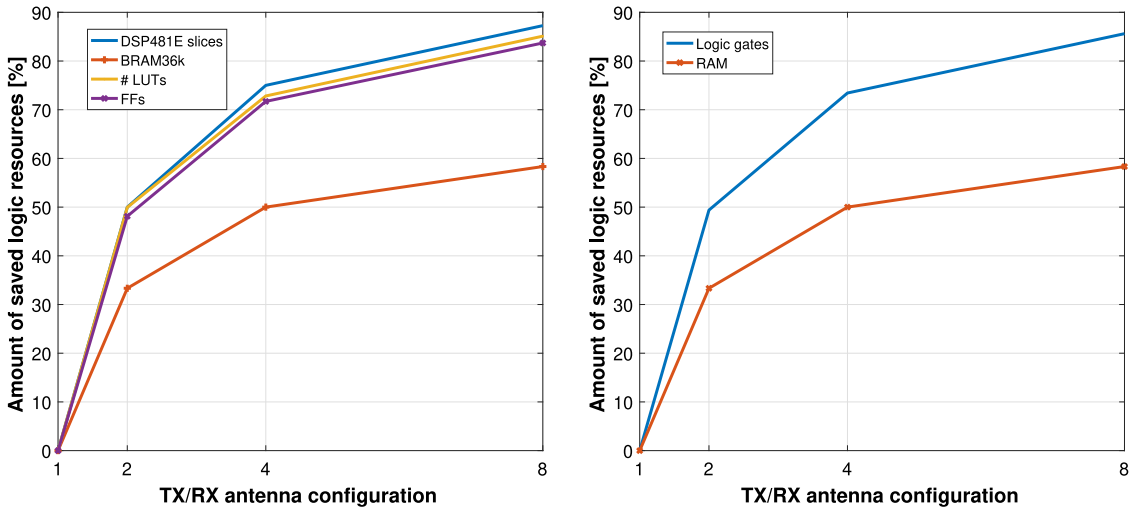
(b)

Fig. 4. Detailed block diagrams of: (a) MUX and (b) DEMUX DSP block algorithm entities, considered in the proposed MIMO–OFDM method.

is illustrated in Fig. 6 for all MIMO configurations. From this figure, it is clearly seen that the utilised logic region does not linearly increase with the number of antennas considered in the MIMO configuration.

Summary of the logical resource utilisation for both conventional and proposed MIMO–OFDM system's implementations is given in Table 2. Results demonstrate that using our MIMO architecture, the number of occupied resources in the FPGA are significantly reduced, when compared with the conventional one. For example, from Table 2, in a 8 × 8 MIMO antenna configuration, only 10.6% of the total VC707 slices capacity is utilised, against 60% in a conventional system implementation. Hence, this method not only successfully reduces the hardware complexity, but also enables a second TRX MIMO-engine branch to be operating in parallel (enabling the system to provide 16 × 16 antenna configurations), considering that two engines would occupy 21.2% of the total number of slices in the VC707. And yet, this value is lower than the 60% verified in the conventional method. This explains the fact that in Fig. 6, the occupied implementation area from the VC707 does not significantly increase with the number of antennas.

Furthermore, results of logic resource usage for the TRX presented in Table 3 can be further detailed into the amount of logic utilised in both TX and RX processing chains, for the MIMO–OFDM system. It is evident that the RX requires much more hardware resources than TX. For example, receiver implementation requires in average more than 70% of slices, LUTs, FFs,



(a) (b)

Fig. 5. Amount of saved logical resources, when using the proposed MIMO design against a conventional one, for 1 × 1, 2 × 2, 4 × 4, and 8 × 8 antenna configurations, considering: (a) resource blocks; and (b) logic gates and RAM.

Table 2
TRX FPGA resources usage for both conventional and proposed MIMO–OFDM methods implementation.

Config.	Method	# of slices	# of LUTs	# of FFs	# of DSP48E1 slices	# of BRAM36ks
1 × 1	Conventional	5683 (7.5%[a])	17 929 (5.9%)	20 635 (3.4%)	54 (1.9%)	42 (4.1%)
	Proposed	5683 (7.5%[a])	17 929 (5.9%)	20 635 (3.4%)	54 (1.9%)	42 (4.1%)
2 × 2	Conventional	11 366 (15%)	35 858 (11.8%)	41 270 (6.8%)	108 (3.9%)	84 (8.2%)
	Proposed	5827 (7.7%)	17 947 (5.9%)	21 410 (3.5%)	54 (1.9%)	56 (5.4%)
4 × 4	Conventional	22 732 (29.9%)	71 716 (23.6%)	82 540 (13.6%)	216 (7.7%)	168 (16.3%)
	Proposed	6707 (8.8%)	19 491 (6.4%)	23 354 (3.8%)	54 (1.9%)	84 (8.2%)
8 × 8	Conventional	**45 464 (60%)**	**143 432 (47.2%)**	**165 080 (27.2%)**	**432 (15.4%)**	**336 (32.6%)**
	Proposed	**8013 (10.6%)**	**21 361 (7%)**	**26 898 (4.4%)**	**55 (1.96%)**	**140 (13.6%)**

[a]Used logic capacity of the VC707, in percentage.

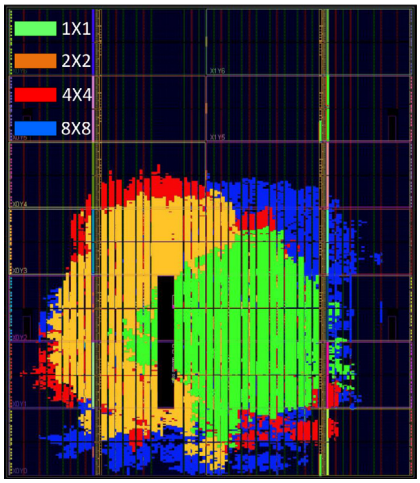


Fig. 6. Occupied hardware footprint for 1 × 1 (SISO), 2 × 2, 4 × 4, and 8 × 8 antenna configurations, in a *Xilinx* Virtex7 XC7VX485T.

DSP48E1 slices in comparison with the TX one. In order to understand this value, Table 4 shows the TX/RX engines breakdown in a 1 × 1 antenna configuration. From this, it can be verified that not only the OFDM demodulator requires almost twice the HW of the TX one. Moreover, the results presented in Table 4 confirm that higher cost units, in terms of logical resources usage, are in both OFDM modulator/demodulator engines, which are precisely the ones that are not replicated in the proposed MIMO–OFDM method.

Finally in Table 5, the TRX MIMO–OFDM power consumption for each antenna configuration is summarised. In this table, *clk_gen_0* and *clk_gen_1* are the two Mixed-Mode Clock Manager (MMCM) blocks utilised for the generation of clocks in the design. Results show that the power consumption required to power up the MIMO–OFDM architecture does not significantly increase with the increasing of the MIMO antenna configurations. This is, 1.4 W are enough to power up the MIMO system for 1 × 1, 2 × 2, 4 × 4, and 8 × 8 antenna configurations. Furthermore, considering that in a 2 × 2 MIMO "worst case" power consumption comparison to traditional OFDM implementations (where it is considered that power consumption scales linearly with the footprint), the proposed architecture presents a power consumption saving of 6%. The total power value for a traditional 2 × 2 MIMO–OFDM architecture was calculated as follows. Firstly, power consumption values of each main unit, given in Table 4, present in the SISO configuration has been divided by two, except for both *clk_gen_0*, and *clk_gen_1* units (their power consumption are approximately the same regardless of the MIMO configuration). Secondly, former values were summed together and its resulting value was multiplied by 2 (number of complete OFDM chains presented at both TX/RX ends).

3.2.2. Processing efficiency

In the above implementation results, the authors were able to boost the clock speed of both TX/RX OFDM engines to 250 MHz,

Table 3
Transmitter and receiver FPGA resources usage for the proposed MIMO–OFDM method implementation.

Array size	TX antenna configuration				
	1	2	4	8	*average*[a] [%]
# of slices	1316 (23.2%[a])	1388 (23.8%)	1755 (26.2%)	2236 (27.9%)	25.3
# of LUTs	3622 (20.2%)	3660 (20.4%)	4231 (21.7%)	4987 (23.3%)	21.4
# of FFs	5642 (27.3%)	5968 (27.9%)	6718 (28.8%)	8155 (30.3%)	28.6
# of DSP48E1 slices	16 (29.6%)	16 (29.6%)	16 (29.6%)	16 (29.1%)	29.5
# of BRAM36ks	19.5 (46.4%)	24.5 (43.8%)	34.5 (41.1%)	54.5 (38.9%)	42.6
Array size	RX antenna configuration				
	1	2	4	8	*average*[a] [%]
# of slices	4367 (76.8%)	4439 (76.2%)	4952 (73.8%)	5777 (72.1%)	74.7
# of LUTs	14 307 (79.8%)	14 287 (79.6%	15 260 (78.3%)	16 374 (76.7%)	78.6
# of FFs	14 993 (72.7%)	15 442 (72.1%	16 636 (71.2%)	18 743 (69.7%)	71.4
# of DSP48E1 slices	38 (70.4%)	38 (70.4%)	38 (70.4%)	39 (70.9%)	70.5
# of BRAM36ks	22.5 (53.6%)	31.5 (56.3%)	49.5 (58.9%)	85.5 (61.1%)	57.5

[a]Average percentage of required logic resources for the TX and RX, from the overall TRX implementation, for each antenna configuration.

Table 4
TX/RX engines resource usage breakdown on a *Xilinx* Virtex7 XC7VX485T FPGA for a SISO antenna configuration.

Main unit	# of slices	# of LUTs	# of FFs	# of DSP48E1 slices	# of BRAM36ks
TX MUX	47	138	109	0	0
OFDM modulator	**1115**	**3312**	**5163**	**16**	**14.5**
TX DEMUX	3	0	4	0	0
RX MUX	3	1	3	0	0
OFDM demodulator	**2189**	**7249**	**9392**	**24**	**13.5**
RX DEMUX	30	82	90	0	0

Table 5
FPGA implementation power consumption for the proposed MIMO–OFDM architecture.

Main unit	Power consumption [mW]			
	SISO	2 × 2	4 × 4	8 × 8
clk_gen_0	115	115	115	115
clk_gen_1	118	117	112	122
FIFOs	69	80	112	167
TX MUX	2	3	5	4
OFDM modulator	**206**	**276**	**325**	**337**
TX DEMUX	1	1	1	1
RX MUX	1	1	2	4
OFDM demodulator	**549**	**617**	**620**	**624**
RX DEMUX	2	2	2	2
Total power	1063	1212	1294	1376

Table 6
TRX processing efficiency.

Implementation technique	B [MHz]	Max. CLK [MHz]	Proc. Eff [%]
Proposed	245.76	250	98.3
Ribeiro [24]	61.44	150	41
Park [40]	40	100	40
Wang [18]	20	220	9
Wu[a] [19]	20	317	6.3

[a]Relation B/clk imposed by the number of IFFT clock cycles required to process data.

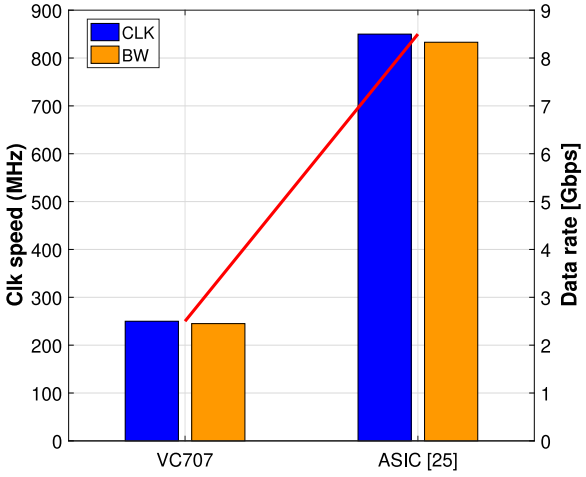


Fig. 7. Comparison of the TRX SISO OFDM performance in terms of clock speed and signal bandwidth by considering both VC707 and ASIC as target hardware platforms.

targeting the LTE maximum sample rate of 30.72 MHz in a 8 × 8 configuration. Such requires a processing load of 14 GMAC/s, which results from a clock rate and a total number of used DSPs equal to 250 MHz and 55 (as shown in Table 2), respectively. This is quite remarkable, since, for example, in the hardware implementation of the MIMO detector in [39], several critical paths of 10 ns are present, which severely limits the design to go beyond the implemented 90 MHz clock. The processing efficiency achieved in the proposed MIMO–OFDM implementation, is assessed in terms of the ratio between maximum clock rate and sample rate, for a 1 × 1 antenna configuration. Results are presented in Table 6, along with a review of the literature on hardware implementation efficiency. From this table, it can be verified that the processing efficiency has been significantly improved, when compared to the work reported in [24], which was the previous state of art. It is a two fold enhancement, where both system clock and bandwidth have been increased from 150 to 250 MHz and from 61.44 to 245.46 MHz, respectively.

Moreover, both maximum clock speed and signal bandwidth results depicted in Table 6, for the proposed MIMO–OFDM implementation, can be further increased by replacing the current target hardware (FPGA) by an ASIC. In fact, FPGA hardware implementations can be relatively easily re-mapped in ASIC, and according to [41], by doing so, clock speeds can be significantly increased by a multiplier factor of 3.4. Therefore, the hardware implementation of the considered TRX MIMO architecture in an ASIC would result in data rate of 8.4 Gbps (836 MHz of aggregated

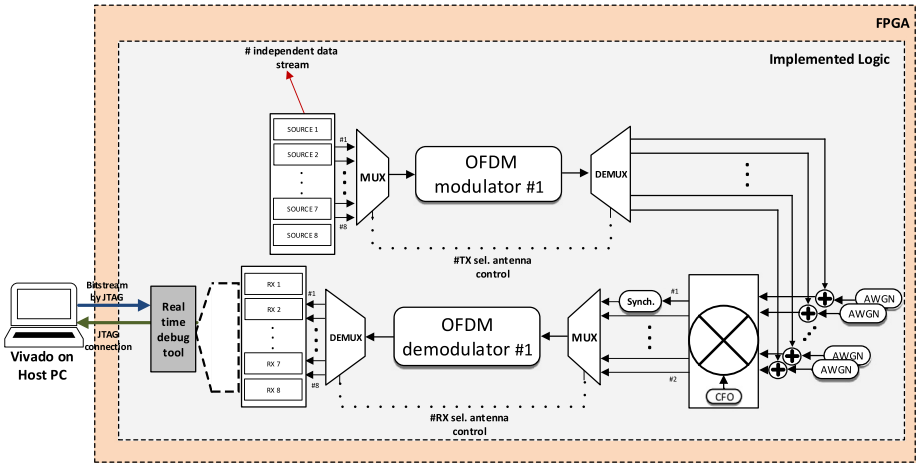
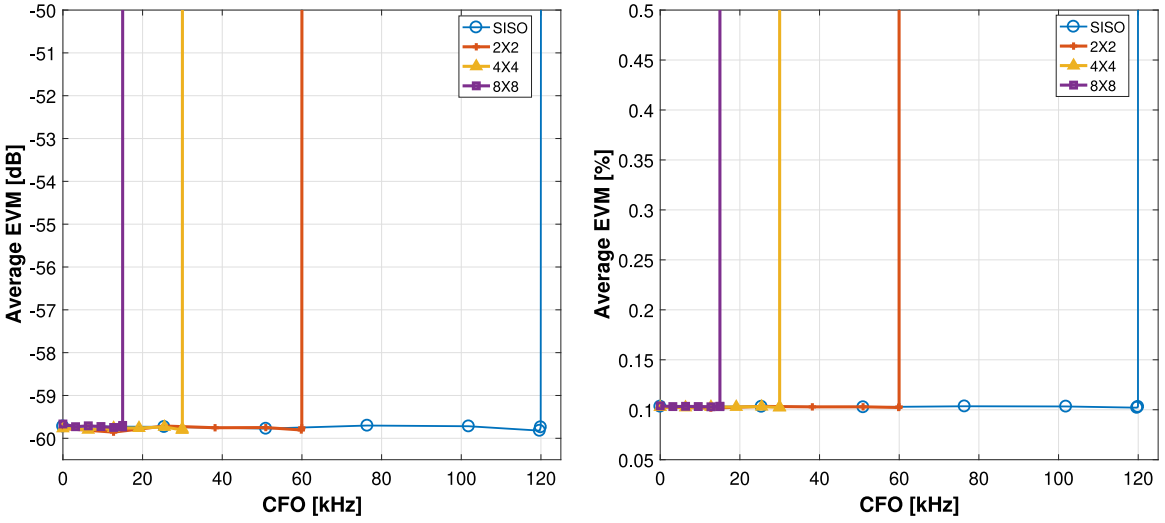


Fig. 8. Block diagram of real-time measurement setup utilised in the system performance assessment.



(a) (b)

Fig. 9. EVM performance of the MIMO–OFDM engine for all antenna configurations, under presence of CFO.

signal bandwidth), considering a 1 × 1 antenna configuration, and employing 1024-QAM, as depicted in Fig. 7. Targeting the LTE's maximum sample rate, a 27 × 27 MIMO configuration would also be enabled by each processing path.

4. Real-time performance assessment of the MIMO–OFDM hardware design

In this subsection, performance of the proposed multi-Gigabit/s MIMO–OFDM TRX architecture (see Fig. 3) in a real-time environment is assessed under the presence of a noisy channel model, using BER and EVM analysis, as performance metrics, for 4-, 16-, 64-, 256-, and 1024-QAM. Additionally, the robustness of the system against CFO is also assessed. This allows to assess whether the proposed architecture induces any degradation on the OFDM performance. Therefore, in addition to those DSP blocks implemented for usage logic resources and FPGA footprint assessment, as illustrated in Fig. 3, a wireless channel and CFO generator blocks were also included in the implemented design. The former was modelled as an AWGN channel, allowing real-time measurements of the BER for different Signal-to-Noise Ratio (SNR) values, while the latter was modelled as an digital IQ mixer (frequency shifter), as depicted in Fig. 8. Mismatch of carrier frequency values are therefore induced by a digital oscillator connected to an IQ mixer, at the receiver. In particular for system performance evaluation, since signals received at all RX antennas are affected by similar delays and CFO values, the joint synch and CFO estimation algorithm only uses the samples from the first antenna, to reduce the HW footprint. Moreover, both decoded bitstream data or equalised QAM constellation symbols are acquired with the aid of a real-time debugging tool.

In an OFDM system, the orthogonality between sub-carriers is only maintained if both the independent LO at the receiver is in synchronism with the one used at the transmitter, and if *Doppler* effect is negligible (i.e., no objects moving in the wireless environment scenario). Otherwise, carrier frequency mismatch will occur at RX, which might result in Inter-Carrier Interference (ICI) and high BER values. To overcome this, such CFO must be estimated and compensated by the receiver. In this work, in order to mitigate this impairment, its value is estimated using the *Beek* algorithm, presented in [24], and it is compensated through the implementation of a CORDIC DSP block, with angular frequency inversely proportional to the estimated CFO value (induced by a structure of parallel IQ mixers). The mathematical expression of

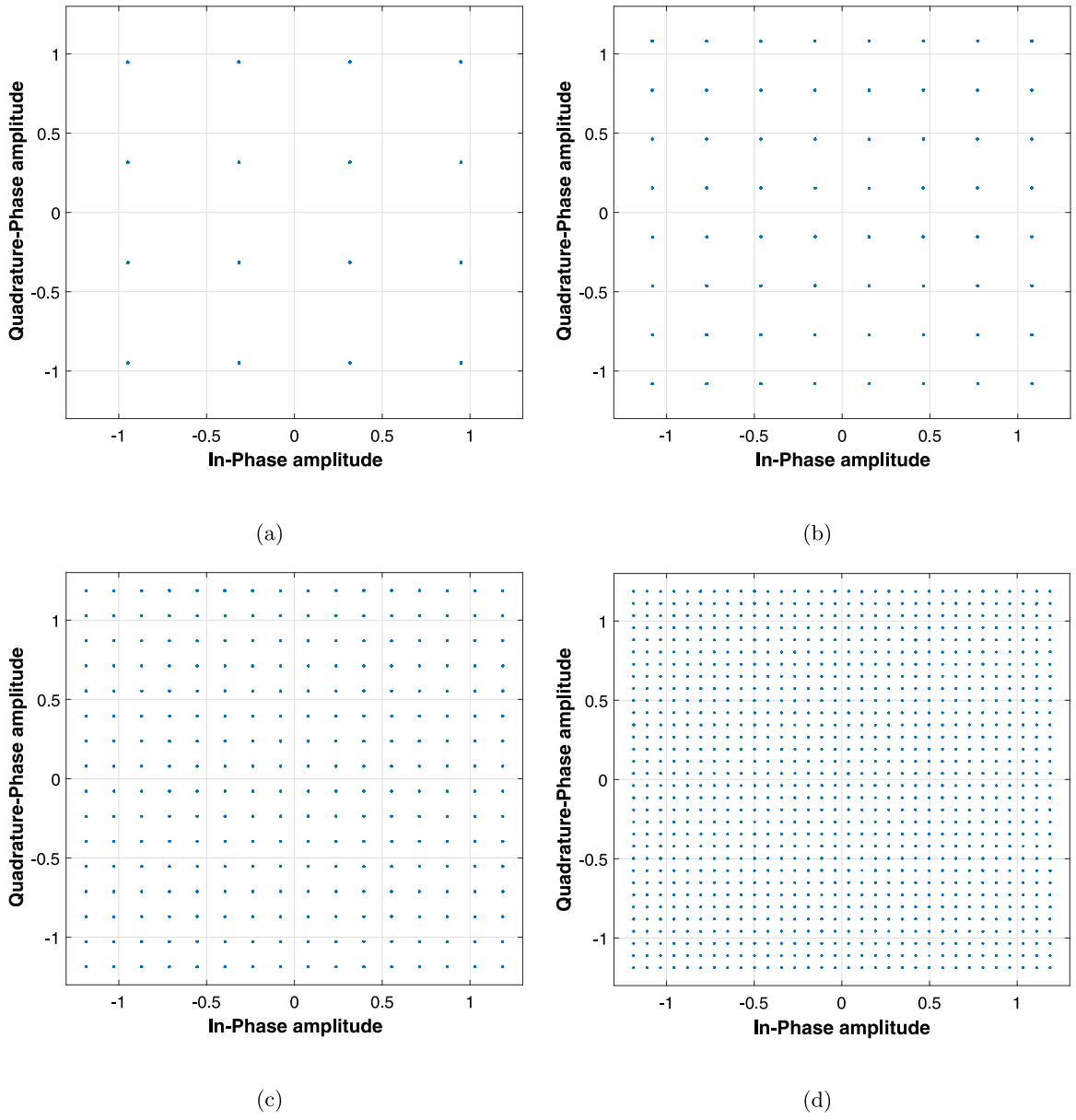


Fig. 10. Received scatter constellation plots, at an $EVM = -60$ dB, for: (a) 16-QAM, (b) 64-QAM, (c) 256-QAM, and (d) 1024-QAM, presented in all MIMO configurations when CFO is compensated.

such operation is given as follows:

$$\begin{aligned} z(n) &= y(n).\exp(-j\omega) = \Big[y_R(n) + jy_I(n)\Big].\exp(-j\omega) \\ &= \underbrace{y_R(n).\cos(-\omega) - y_I(n).\sin(-\omega)}_{\text{In-Phase}} + \\ &\quad \underbrace{y_R(n).j\sin(-\omega) + y_I(n).j\cos(-\omega)}_{\text{Quadrature-Phase}}, \end{aligned} \tag{1}$$

where n is the sample index of each frame, $z(n)$, is the CFO compensated signal, and y_R, y_I are the OFDM received real and imaginary signal parts, respectively. The estimated angular frequency (ω) is given by $2.\pi\epsilon.n$, where ϵ, is the rotation angle obtained by the *Beek* algorithm, which is then accumulated along each received OFDM symbol.

Fig. 9 shows the measured average EVM values for each MIMO–OFDM configuration under the presence of CFO. From these results, it is clearly demonstrated that the considered MIMO TRX system can deal with relatively high range of carrier frequency offsets, and that the boundaries of the CFO estimation algorithm, for the different MIMO configurations, are not being affected by the proposed implementation. This is, the acquisition range of the joint Maximum Likelihood (ML) estimator of time and CFO algorithm reported in [37], for OFDM systems, is limited to half of the symbol sub-carrier spacing, which is in line with the results obtained in Fig. 9. In this context, the higher the number of antennas in the MIMO configuration, the lower is the maximum CFO value the system can deal with. On one hand, a SISO configuration, where sub-carrier spacing is 240 kHz, can deal with CFO values up to 120 kHz with no performance degradation (EVM values are always around -60 dB (0.1%)). Such value is the result of imperfections in the RX OFDM engine algorithms, such as channel estimation and equalisation [24], and the consideration of a limited data bus width. On the other hand, a 8×8 MIMO configuration can only compensate CFO values up to 15 kHz. Nevertheless, this value does not represent a significant design limitation in transmissions over-the-air. For example,

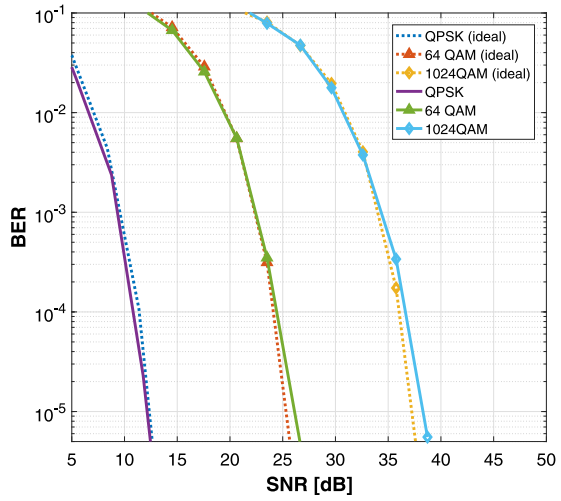


Fig. 11. BER performance of the MIMO–OFDM engine for all antenna configurations, considering 4-, 64-, and 1024-QAM.

within such CFO compensation range, the proposed system is not only able to support the maximum mobility requirement of LTE-Advanced (500 km/h) [42], but also enables a range of 13.33 (15−1.67) kHz, where 1.67 kHz represents the maximum *Doppler* effect value, at a carrier frequency of 3.6 GHz, to compensate possible CFO values at RX induced by TX/RX frequency mismatch.

Furthermore, as it can be seen in Fig. 10, when carrier offset mismatch is compensated, 16-, 64-, 256- and 1024 QAM constellations do not present significant scattering distortion on the received symbols. This subjective quality evaluation indicates that the proposed MIMO architecture is very accurate, remarkably showing potential for 4096-QAM implementations, since the scatter points are visible well separated the 1024-QAM constellation.

Measured BER results have been computed for 1×1, 2×2, 4×4 and 8×8 OFDM MIMO configurations, for 4-, 64-, and 1024-QAM orders. A comparison between these values and those obtained from the theoretical expression, given in (2) [43], for OFDM transmissions over AWGN channels, has also been considered. From Fig. 11, results exhibit a good match with the theoretical ones (dash lines), in which the small gap between both lines can be attributed to the limited 22-bit fixed-point bus format resolution adopted in the hardware design. In fact, this was found the best trade-off between the minimum usage of DSP48E1 slices in the FPGA design and with of the data bus. Higher number of bits per bus would result in the use of more than one DSP48E1 slice per multiply and accumulate operations, which would lead to an increased power consuming and more complex HW design.

$$\mathrm{BER}_{\mathrm{AWGN}} = \frac{2(M-1)}{M\log_2(M)} Q\left(\sqrt{\frac{6E_b}{N_o}\frac{\log_2(M)}{M^2-1}}\right), \tag{2}$$

where, M is the modulation order, E_b/N_o is the energy per bit to noise power spectral density ratio and $Q(.)$ is the standard Q-function. Converting to SNR to E_b/N_o is performed according to: $\mathrm{SNR}[dB] = E_b/N_o[dB] + 10\log_{10}(k)$, where k, is the number of information bits per symbol.

5. Conclusion

In this paper, a novel method for hardware efficient MIMO–OFDM designs is presented for 1×1, 2×2, 4×4, and 8×8 antenna configurations, and implemented in a VC707 *Xilinx* FPGA. To the best of authors' knowledge, the most relevant MIMO architectures require one pair of IFFT/FFT per antenna, which might lead to enormous amount of digital processing resources and energy consumption, particularly in massive MIMO configurations. To this extent, the proposed MIMO architecture has been developed to fulfil the gap of efficient MIMO HW designs present in the literature.

The proposed MIMO–OFDM system efficiently utilises a fully pipelined modular architecture with a processing efficiency of over 98.3%, (to the best of the authors' knowledge it goes significantly beyond the state-of-the-art). Due to its ability to reduce the design timing constraints, a maximum clock speed of 250 MHz has been achieved in the VC707 implementation. Additionally, it has been demonstrated that the proposed architecture re-uses the most HW consuming DSP algorithms present in a MIMO–OFDM architecture. Sharing the transceiver chain resources among all antenna paths reduces more than 87% hardware in terms of DSP48E1 slices, when compared with conventional design methods. This allows, for example, the implementation of 2 parallel MIMO–OFDM engines in a single *Xilinx* Virtex7 XC7VX485T FPGA, enabling the deployment of a 16×16 MIMO antenna configuration, fulfilling LTE maximum signal bandwidth, resulting in a complete 5 Gigabit/s wireless communication system.

Moreover, it has been demonstrated through RT EVM measurements, that the proposed MIMO–OFDM TRX has negligible system performance degradation in presence of CFO, with an EVM always below −60 dB. The receiver is able to compensate CFO values up to 15, 30, 60, and 120 kHz, for 8×8, 4×4, 2×2, and 1×1, antenna configurations, respectively. Furthermore, experimental BER curve results of MIMO–OFDM transmissions over an AWGN channel, are very close to the ideal ones, which proves that a 22-bit bus format is a good compromise between both system complexity and performance.

Finally, the presented work in this paper might be an important guide to establish RT massive MIMO links over the air in future 5G wireless communication systems, at the minimum expense of hardware resources. The proposed architecture is flexible to be scalable to hundreds of antenna paths, at both radio ends, depending on the footprint of the target integrated circuit, which might enable the deployment of phantom cells envisaged for the 5G network. Therefore, time for evaluation and validation of new MIMO coder/decoder envisaged for future wireless communications systems might be significantly reduced, when using the suggested MIMO architecture.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

CRediT authorship contribution statement

Carlos Ribeiro: Conceptualization, Methodology, Software, Data curation, Writing - original draft, Visualization, Investigation, Validation, Writing - review & editing, Supervision. **Rodolfo Gomes:** Conceptualization, Methodology, Software, Data curation, Writing - original draft, Visualization, Investigation, Validation, Writing - review & editing. **Luís Duarte:** Conceptualization, Methodology, Software, Data curation, Writing - original draft, Visualization, Investigation, Validation, Writing - review & editing. **Akram Hammoudeh:** Conceptualization, Methodology, Software, Data curation, Writing - original draft, Visualization, Investigation, Validation, Writing - review & editing, Supervision. **Rafael F.S. Caldeirinha:** Conceptualization, Methodology, Software, Data curation, Writing - original draft, Visualization, Investigation, Validation, Writing - review & editing, Supervision.

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